

MODEL NAME : AAP01
PROJECT CODE : ANRAAP0100
PCB NO :
DAA000AK000 LA-C901P M/B
DA400237000 LS-C901P SSD/B
DA40023X000 LS-C902P SSD/B (w/o redriver)
DA40023Y000 LS-C904P LOGO/B

ZZZ PCB@
PCB 1FU LA-C901P REV0 M/B MLK 3
DAA000AK000

ZZZ PCBR1@
PCB 1FU LA-C901P REV1 M/B MLK 3
DAA000AK010

ZZZ PCBR3@
PCB 1FU LA-C901P REV1 MB MLK TRIP 3 A31!
DAA000AK011

ZZZ DAZR1@
PCB AAP01 LA-C901P LS-A302P/A303P/C904P 02
DAZ1FU00100



HDMI@ ROYALTY HDMI W/LOGO	
Part Number	Description
R0000000020M	HDMI W/Logo:R0000000020M

Layout Dell logo



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ALL RIGHT RESERVED
REV: X00
PWB: XXXXX
DATE: 1450-06

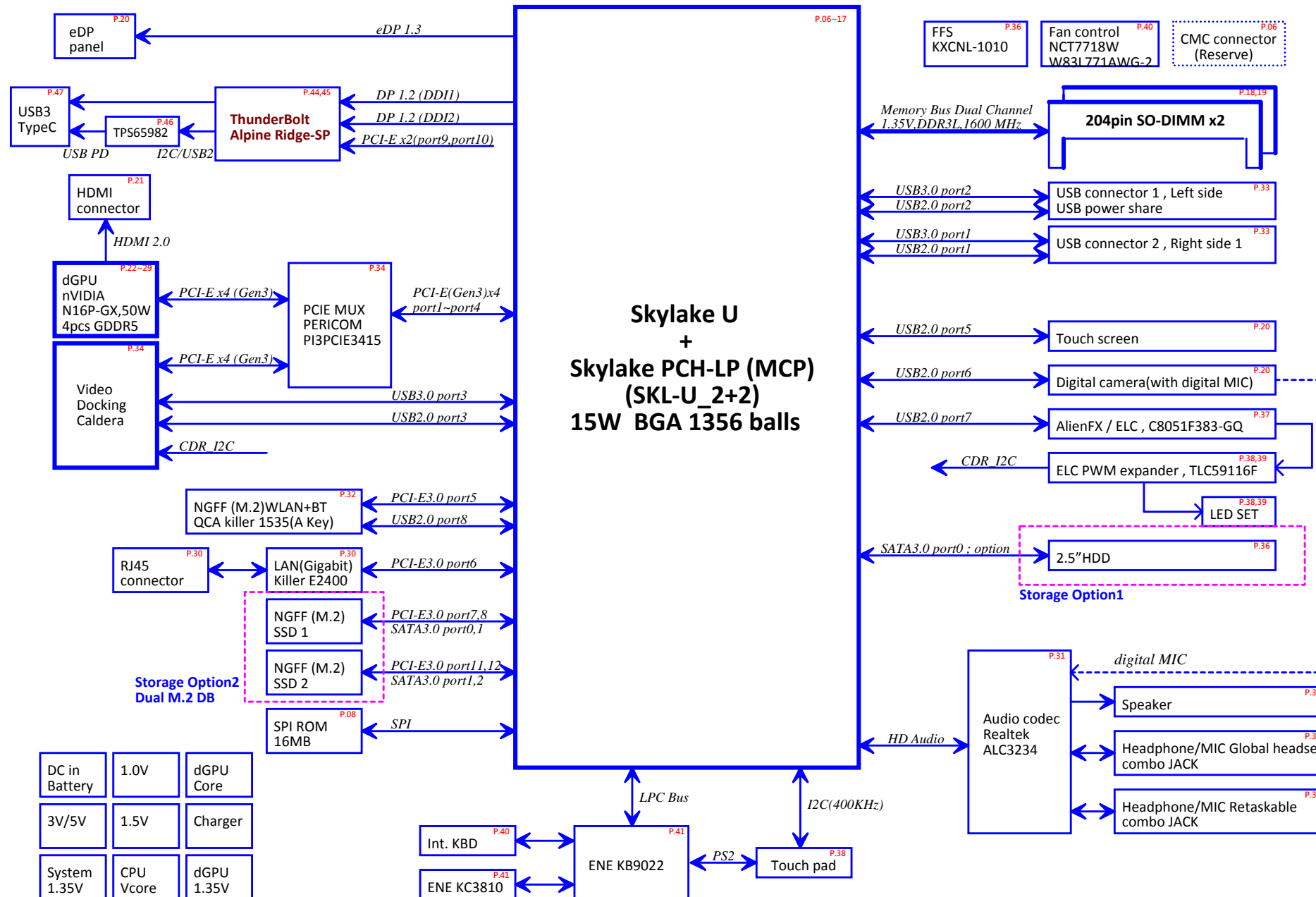
Echo MLK 13" SKL-U
Skylake U-type (1 chip_DSC)

REV : 1.0 (A00)

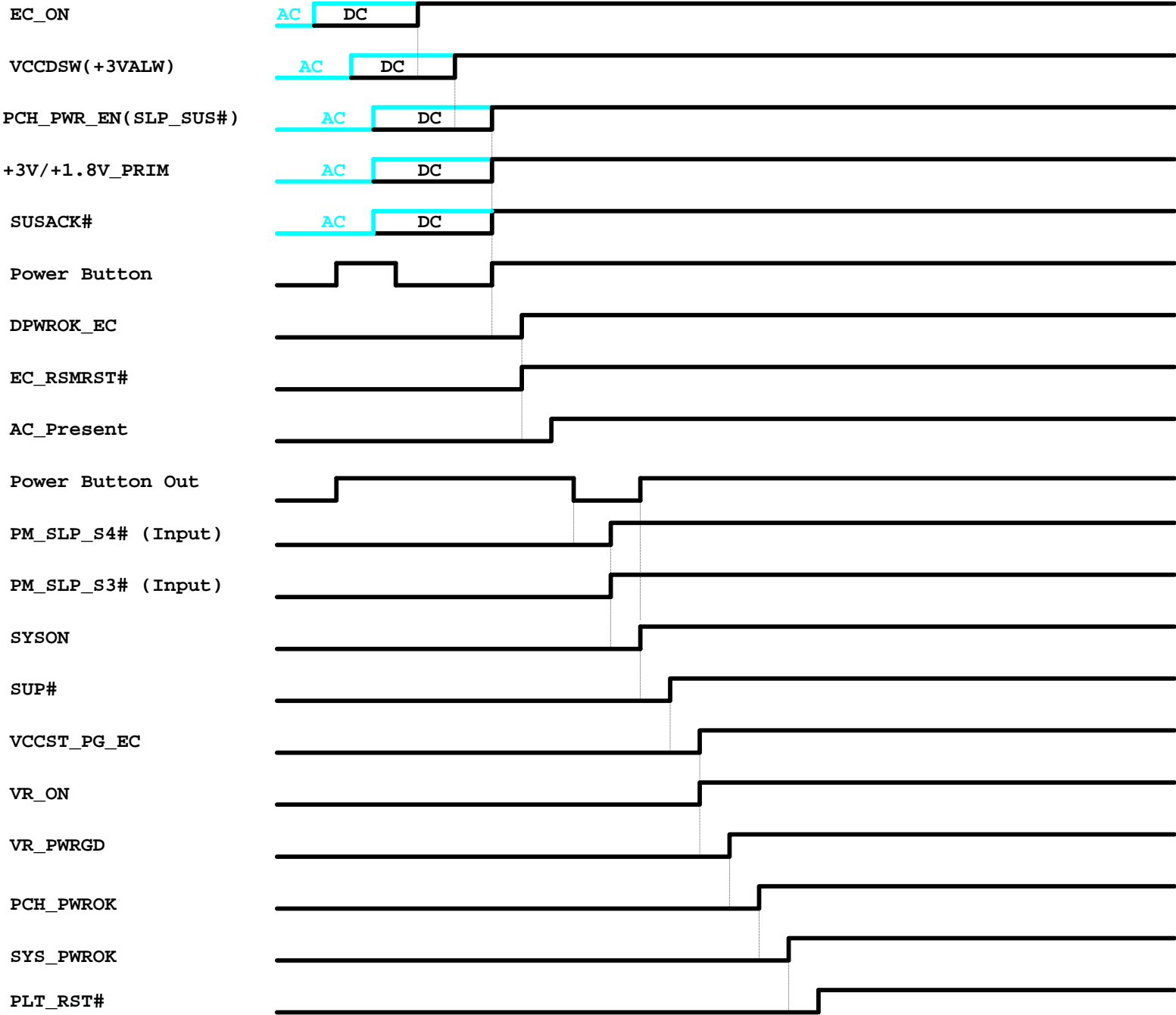
2015.07.14

@ : Nopop Component
EMI@,ESD@ : EMI/ESD/RF part
CONN@ : Connector Component
CMC@ : Total debug Component

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				Rev	1.0



Power on sequence



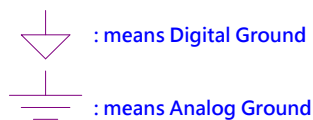
Board ID Table for AD channel

Vcc	3.3V				
Ra	100K +/- 1%				
Board ID	Rb	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	EC AD3
0	0		0.000V	0.300V	0x00 - 0x13
1	12K +/- 1%	0.347V	0.354V	0.360V	0x14 - 0x1E
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1F - 0x25
3	20K +/- 1%	0.541V	0.550V	0.559V	0x26 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3A
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3B - 0x45
6	43K +/- 1%	0.978V	0.992V	1.006V	0x46 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA4
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA5 - 0xAF
13	240K +/- 1%	2.316V	2.329V	2.343V	0xB0 - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xBF
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC0 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD4
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD5 - 0xDD
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDE - 0xF0
19	NC	3.000V	3.000V		0xF1 - 0xFF

Board ID table and PCB version

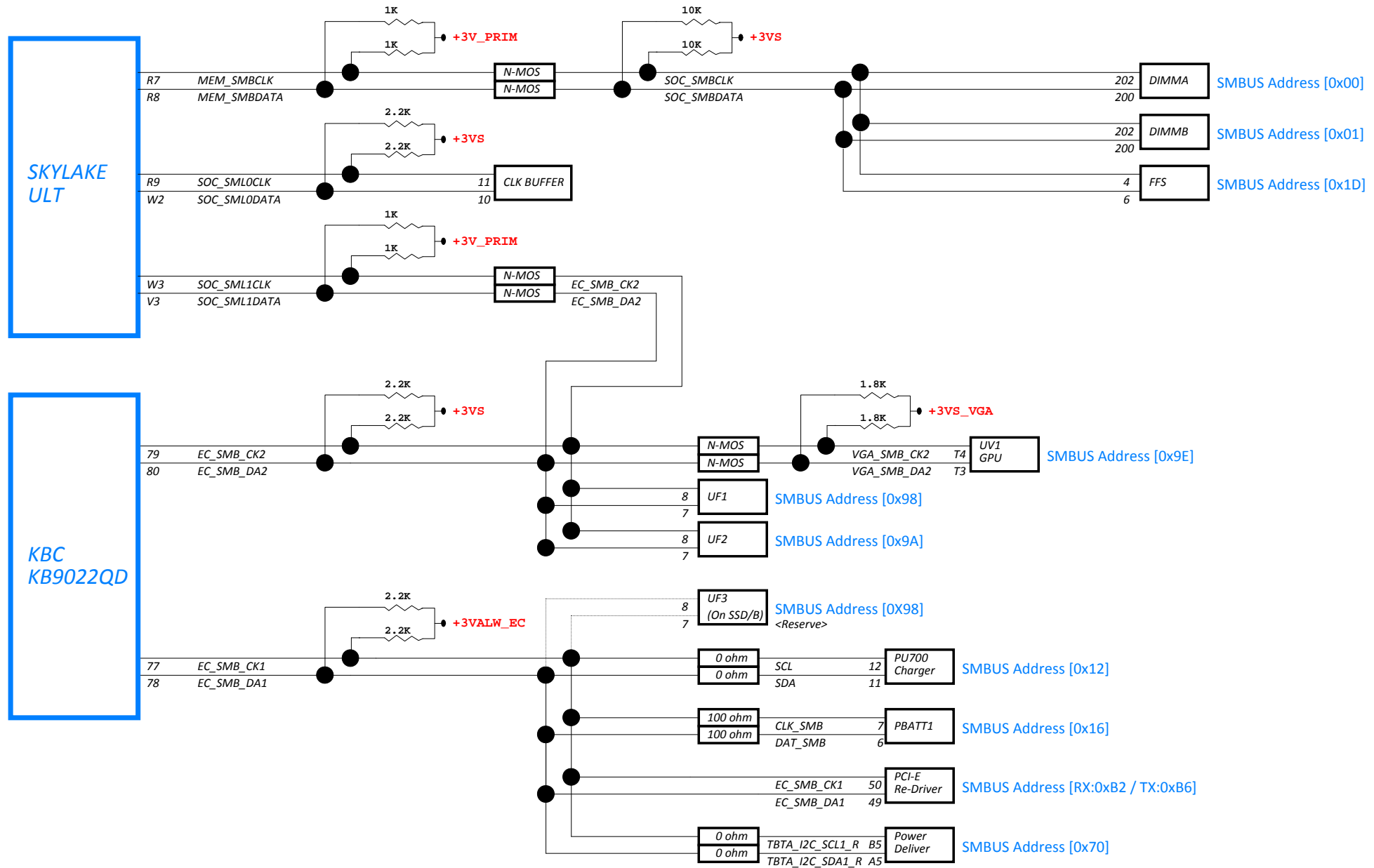
ID	Rb		
0	0	EVT(R0.1)	
1	12K	DVT-1(R0.2)	
2	15K	DVT-1.1(R0.3)	
3	20K	DVT-2(R0.4)	
4	27K	Pilot(R1.0)	
5	33K		
6	43K		
7	56K		

Symbol Note :



CLOCK SIGNAL	
CLKOUT_PCIE0	N16P-GX +Caldera
CLKOUT_PCIE1	M.2 Card WLAN+BT
CLKOUT_PCIE2	Giga LAN
CLKOUT_PCIE3	M.2 NGFF SSD
CLKOUT_PCIE4	Thunderbolt
CLKOUT_PCIE5	M.2 NGFF SSD

ULT	USB3.0	
	Port1	Right side 1
	Port2	Left side (power share)
	Port3	Caldera
	Port4	
	USB2.0	
	Port1	Right side 1
	Port2	Left side (power share)
	Port3	Caldera
	Port4	
	Port5	Touch screen
	Port6	Camera
	Port7	ELC
	Port8	BT
	PCI EXPRESS	
	Lane 1~4	MUX for dGPU & Caldera
	Lane 5	WLAN(M.2 Card)
	Lane 6	10/100/1000 LAN
	Lane 7~8	M.2 SATA+PCIeX2
	Lane 9~10	Alpine Ridge SP
	Lane 11~12	M.2 SATA+PCIeX2
	SATA	
	SATA0	HDD or SSD1
	SATA1	SSD2
	SATA2	SSD2
	SATA3	



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S IC A31 FJ8066201924932 QHMG C0 1.6G S IC A31 FJ8066201924925 QHMF C0 2.3G
SA00008M30L SA00008M40L
1.6GES@ 2.3GES@

UC1 I5-6200U UC1 I7-6500U
S IC A31 FJ8066201930409 QJ8N D0 2.3G S IC A31 FJ8066201930408 QJ8L D0 2.5G
SA00009200L SA000092P0L
1.6GES@ 1.7GES@

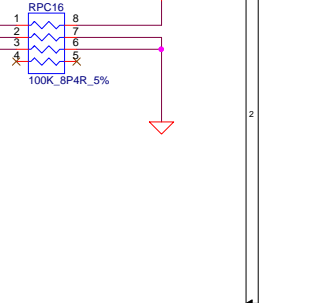
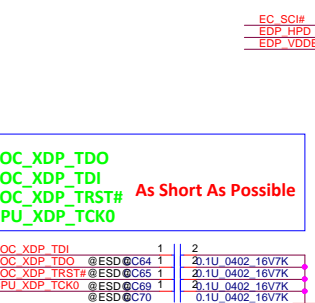
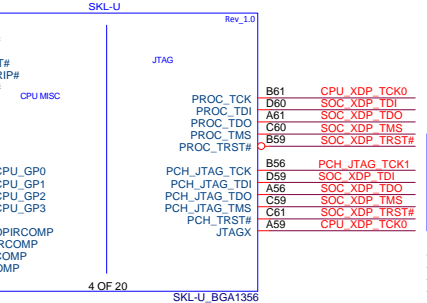
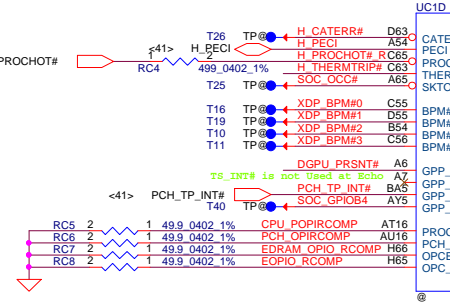
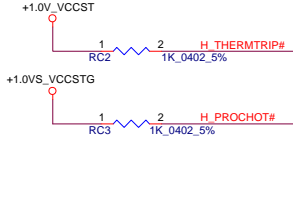
UC1 I5-6200U UC1 I7-6500U
S IC A31 FJ8066201930409 QJ8N D1 2.3G S IC A31 FJ8066201930408 QJ8L D1 2.5G
SA00009201L SA000092P1L
1.6GES@ 1.7GES@

UC1 I5-6200U UC1 I7-6500U
S IC FJ8066201930409 SR2EY D1 2.3G A31 S IC FJ8066201930408 SR2EZ D1 2.5G A31
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1.6GES@ 1.7GES@

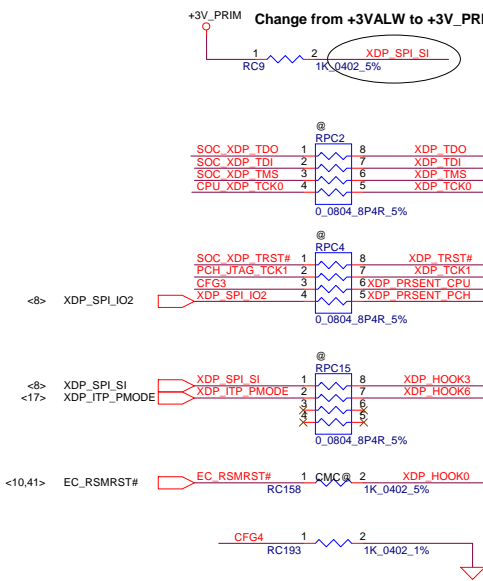
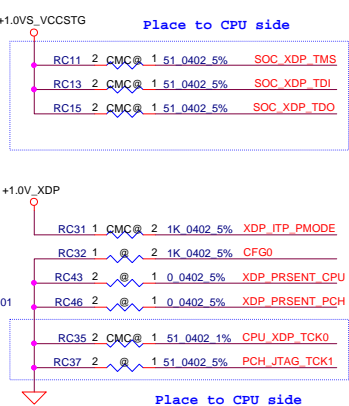
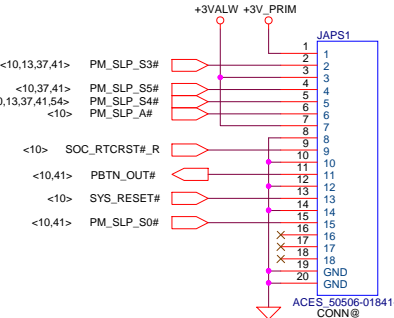
For BIOS Verify UMA/DIS SKU

UMA# DGPU_PRST#

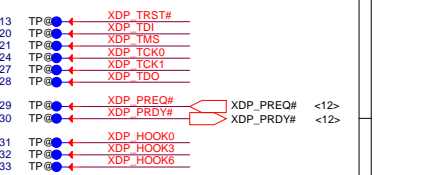
GPP_E15	DGPU_PRST#
DIS,Optimus	0
UMA	1



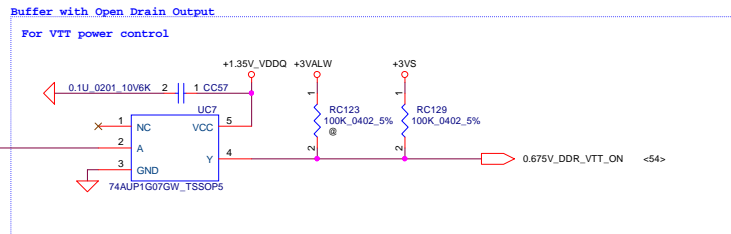
APS CONN



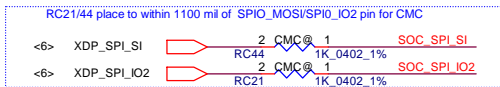
PRIMARY CMC CONN



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Title			
SKL-U(2/12)DDRIII			
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SOC_SMBALERT#

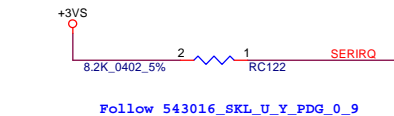
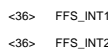
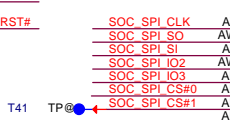
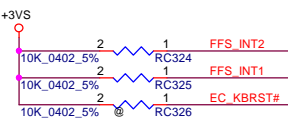
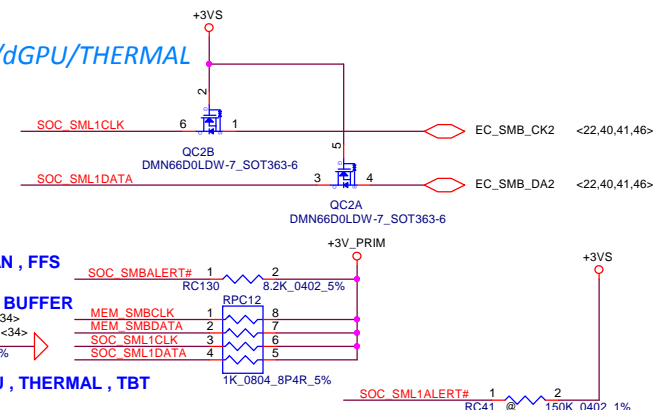
TLS CONFIDENTIALITY	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

SOC_SML0ALERT#

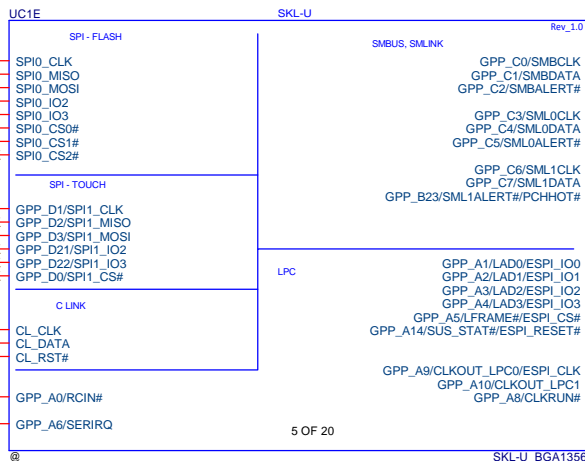
EC interface	
HIGH	ESPI
LOW(DEFAULT)	LPC

----->For KB9032 Only.
----->For KB9022/9032 Use

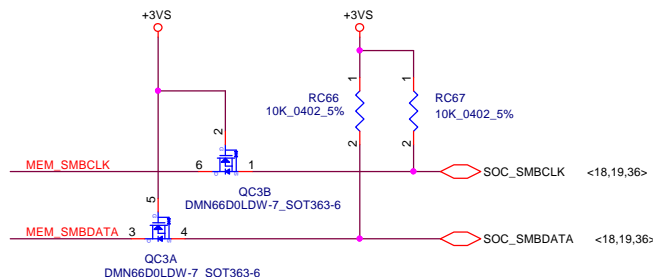
SML1 Bus : EC/dGPU/THERMAL



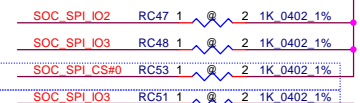
Follow 543016_SKL_U_Y_PDG_0_9



SMB Bus : DDR/WLAN/FFS



Reserve For EC Auto Load Code



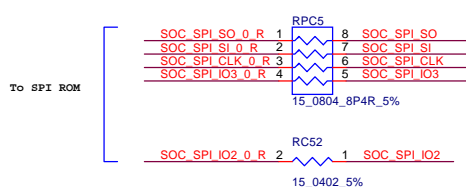
*****ONLY*****
From WW36 MOW for SKL-U ES sample



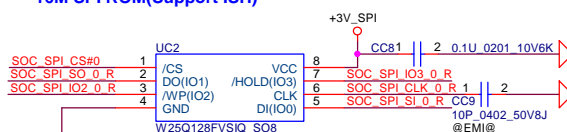
Follow TD team

Single SPI ROM_CS0#

RPC5 and RC52 are close UC2

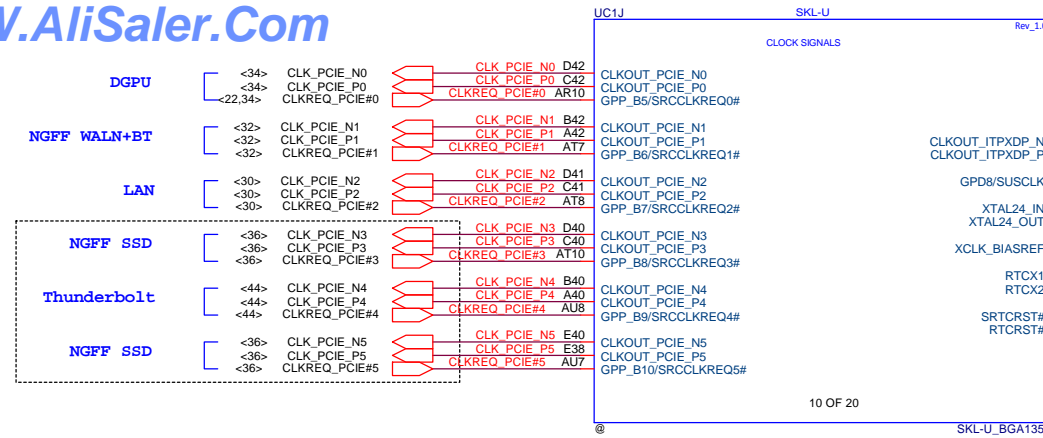


16M SPI ROM(Support ISH)

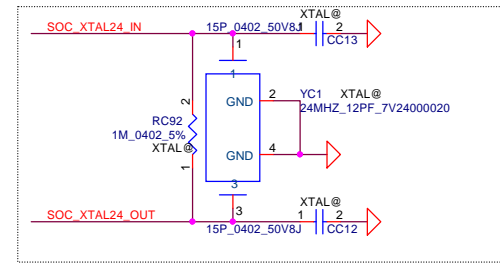


SPI ROM Setting	Bom Option
8M + 2M (Standard Demand)	Single SPI = 2M_SINGLE@(UC2) Dual SPI = 8M_DUAL@
8M + 4M(If Support ISH)	Single = 4M_SINGLE@(UC2) Dual SPI = 8M_DUAL@
8M + 8M(If Support ISH+VPRO)	Single = 8M_SINGLE@(UC2) Dual SPI = 8M_DUAL@
16M	Single = 16M_SINGLE@ (UC2)

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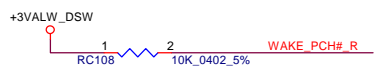
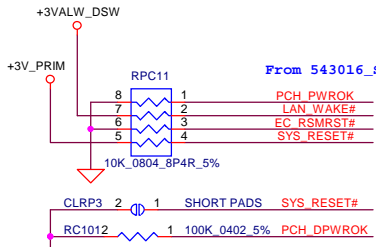
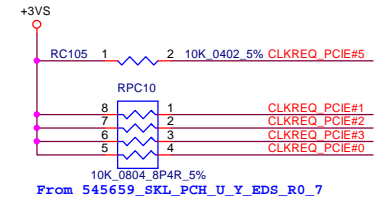
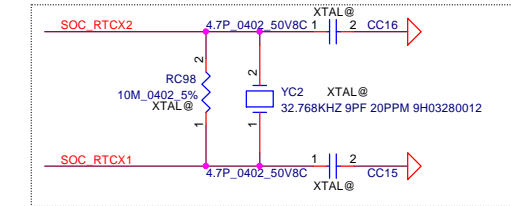


****Avoid Sub-trace****
Closed to CPU

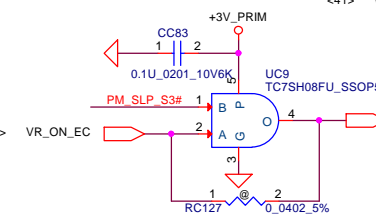
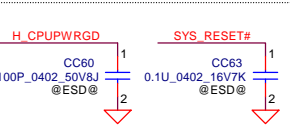


****Avoid Sub-trace****

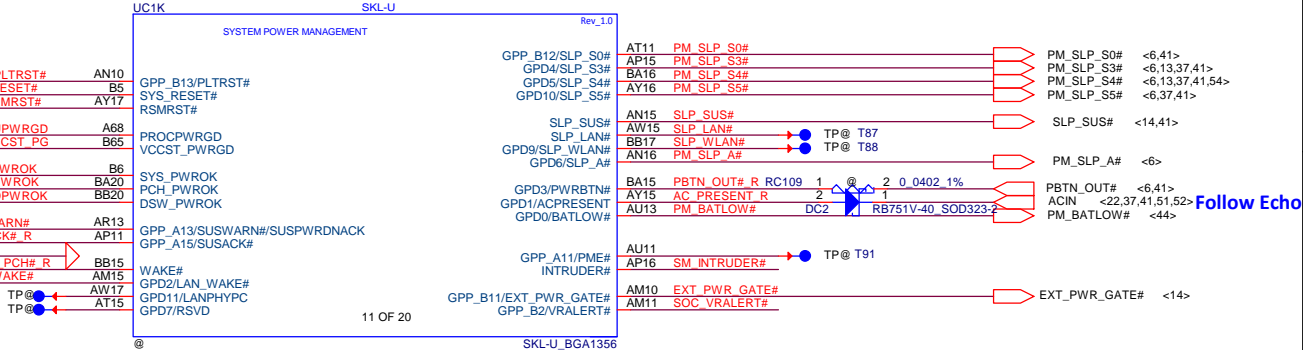
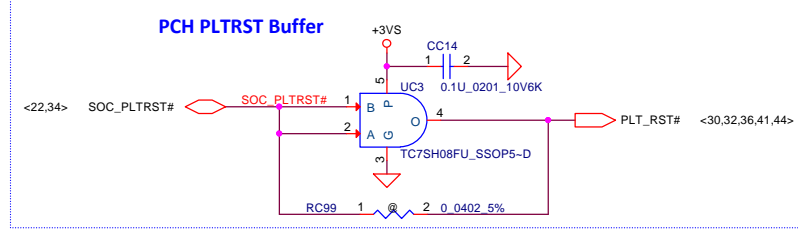
Closed to CPU



EC_VCCST_PG
H_CPUPWRGD As Short As Possible
SYS_RESET#

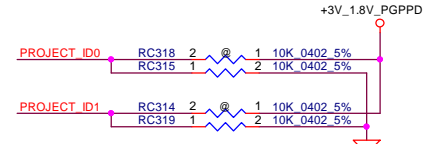
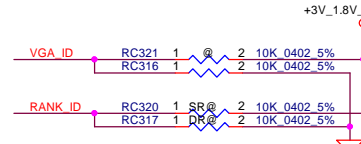
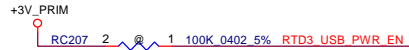
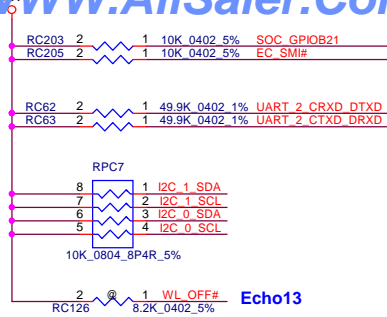


For meet tPLT17 & tCPU28 power down sequence.
tPLT17 : 1us (Max)
tCPU28 : 1us (Max)



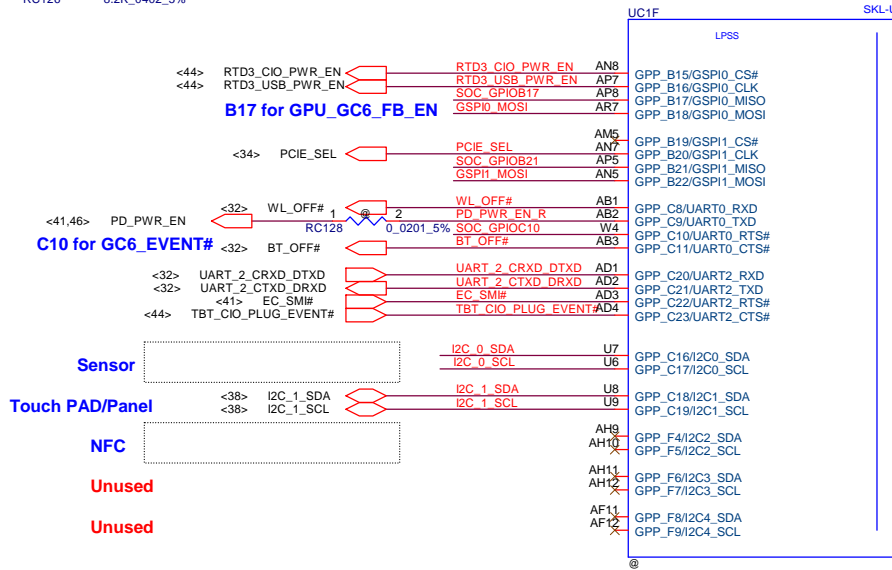
Follow Echo

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VGA_ID	GPP_D9	RANK_ID	GPP_D10
GL	0	DR	0
GM	1	SR	1

Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
*Project code	0	0
Reserved	0	1
Reserved	1	0
Reserved	1	1



Sensor
Touch PAD/Panel
NFC
Unused
Unused

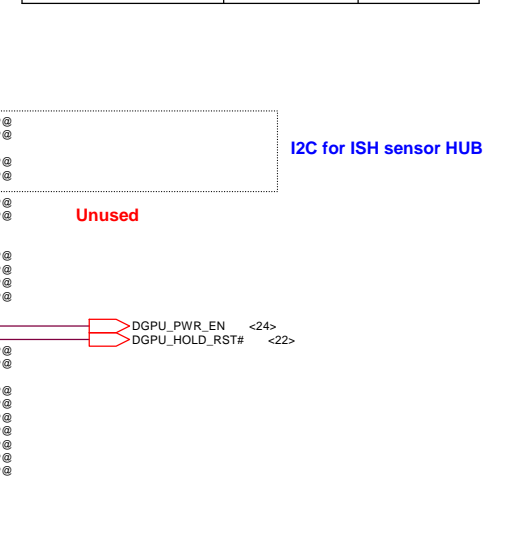
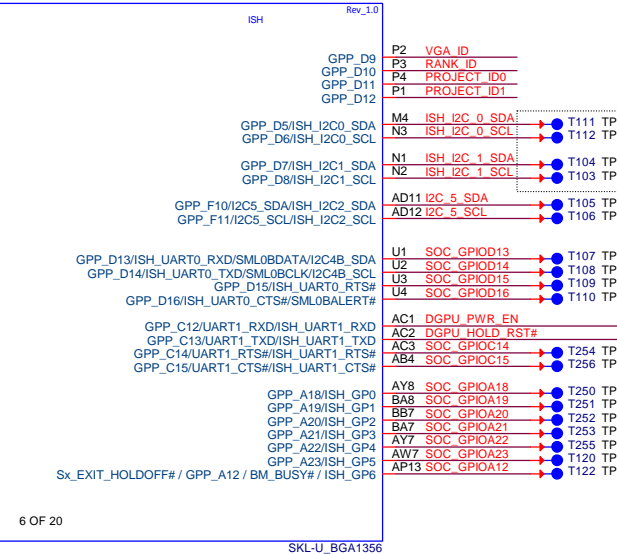
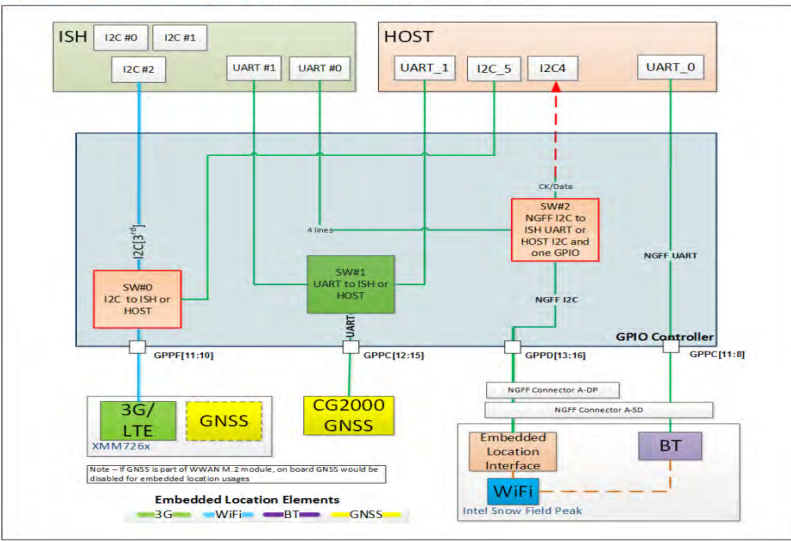
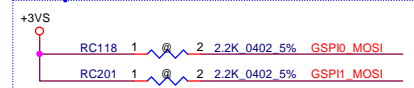


Figure 64-1. Embedded Location - Host and ISH Connectivity



Strap Pin



GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. --> AAX05 Use

1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running JTP/XDP.

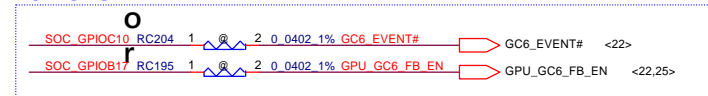
GSPI1_MOSI (Internal Pull Down):

Boot BIOS Strap Bit

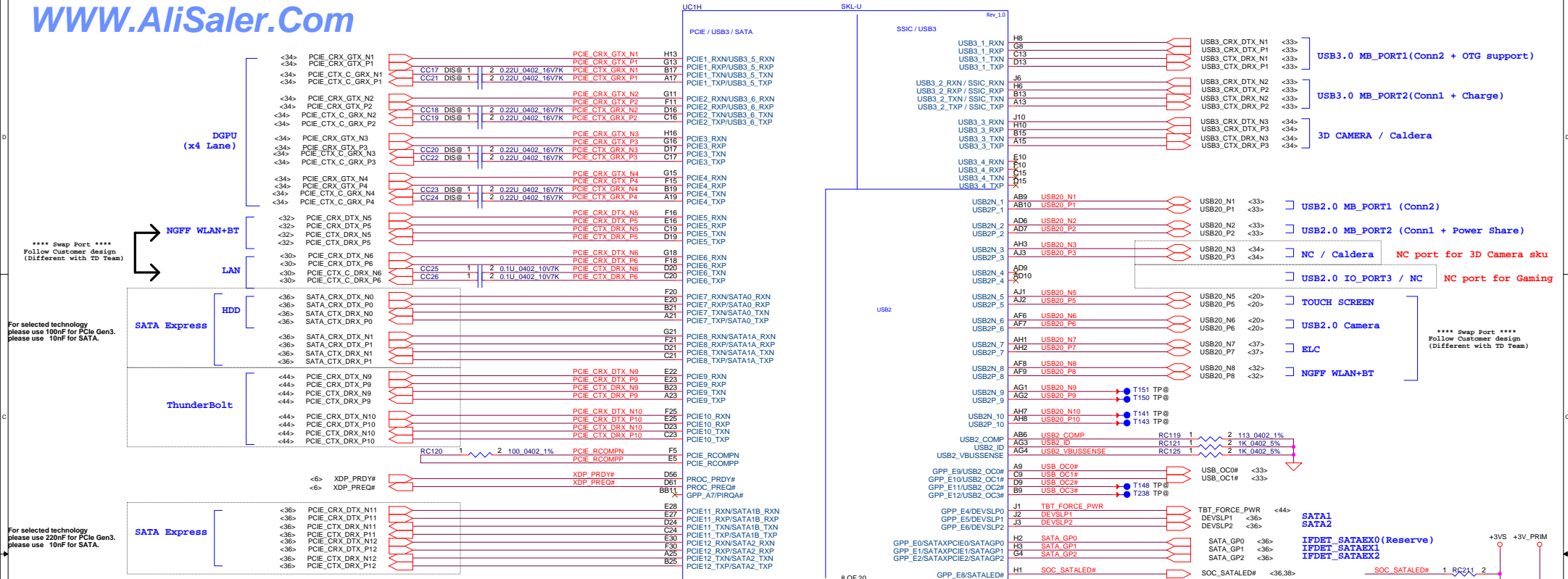
0 = SPI Mode --> AAX05 Use

1 = LPC Mode--> AAP01 Use

TO DGPU

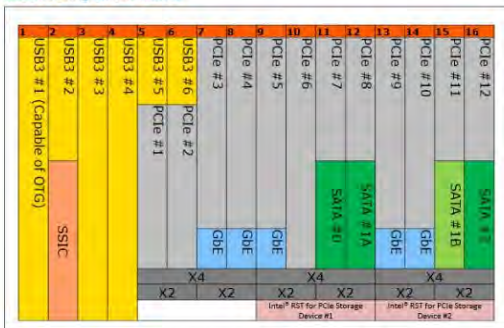


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Compal Electronics, Inc.		Title	
SKL-U(6/12)GPIO		Size	
LA-C901P		Rev 1.0	
Date: Tuesday, August 04, 2015		Sheet 11 of 63	



3.4.1 SKL PCH U Flexible I/O

Figure 3-1. HSIO Muxing on SKL PCH U



- Up to 12 PCIe* lanes (multiplexed with USB 3.0 ports, SATA Ports)
 - Only a maximum of 6 PCIe* ports (or devices) can be enabled at any time.
 - Ports 1-4, Ports 5-8, and Ports 9-12, can each be individually configured as 4x1, 2x2, 1x2 + 2x1, or 1x4.
- Up to 3 SATA ports (multiplexed with PCIe*)
 - SATA Port 1 has the flexibility to be mapped to either PCIe* Port 8 or Port 11.
- Up to 6 USB 3.0 ports (multiplexed with PCIe*)
 - USB Dual Role (OTG) capability is available on USB 3.0 Port 1
 - One SSIC x1 port is multiplexed with USB 3.0 Port 2
- One GbE lane
 - GbE can be mapped into one of the PCIe* Ports 3-5 and Ports 9-10
 - When GbE is enabled, there can be at most up to 5 PCIe* ports enabled.
- Up to 2 Intel RST for PCIe* storage devices supported
 - Devices can be x2 or x4
 - Devices can be implemented on PCIe Ports 5-8 and Ports 9-12

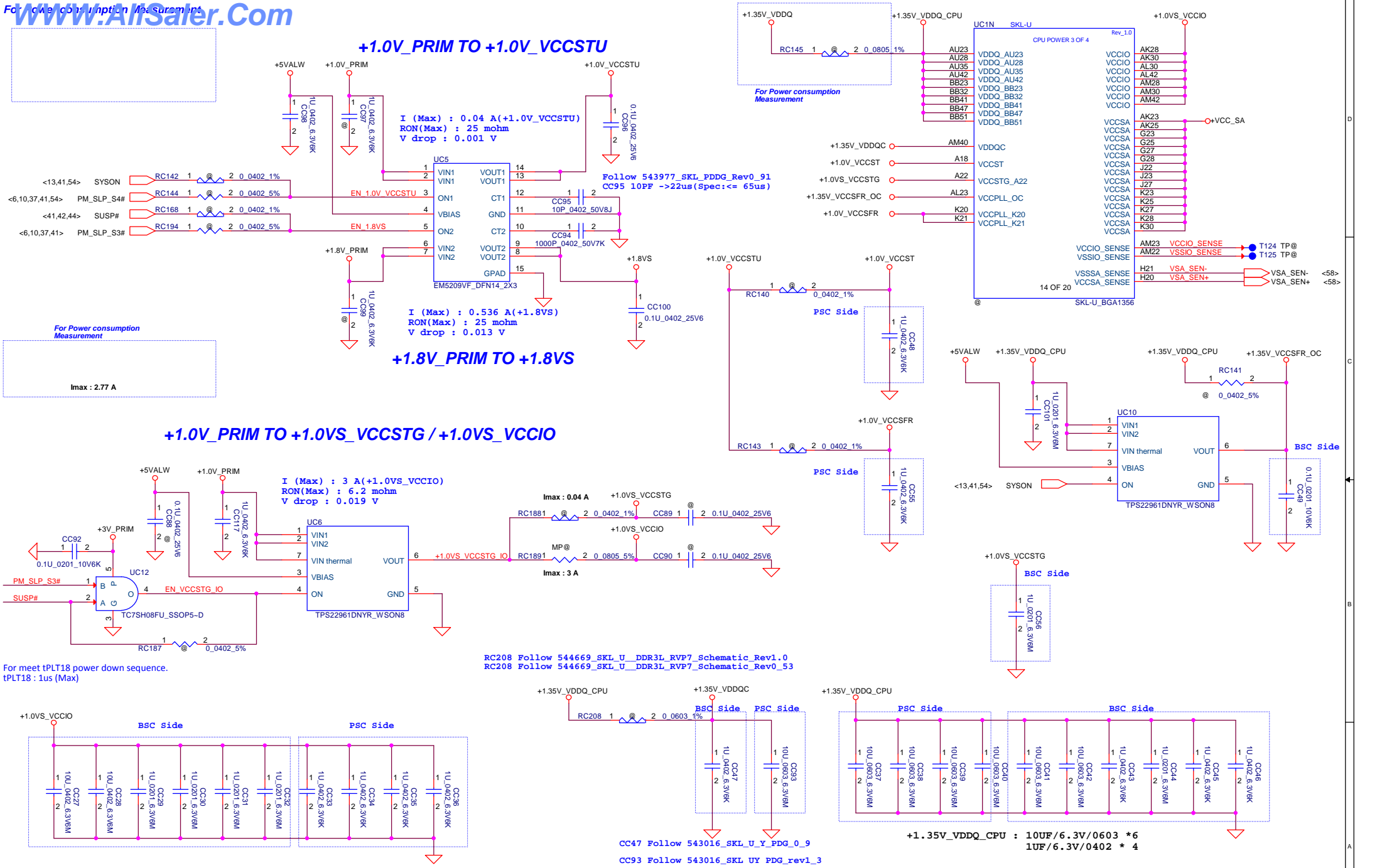
When PCIe8/SATA1A is used as SATA Port 1 (ODD), then PCIe11/SATA1B (M.2 SSD) cannot be used as SATA Port 1.

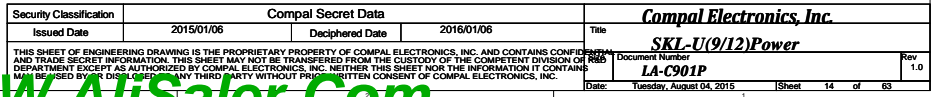
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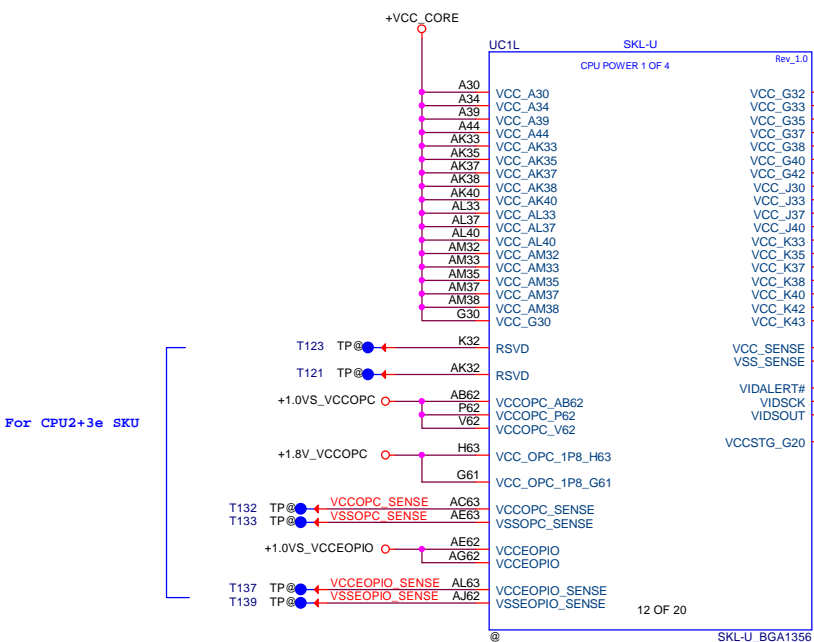
Table 1-3. PCH-LP HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	SATA	SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A
Premium-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	PCIe/ SATA	PCIe/ SATA
Premium-Y	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A

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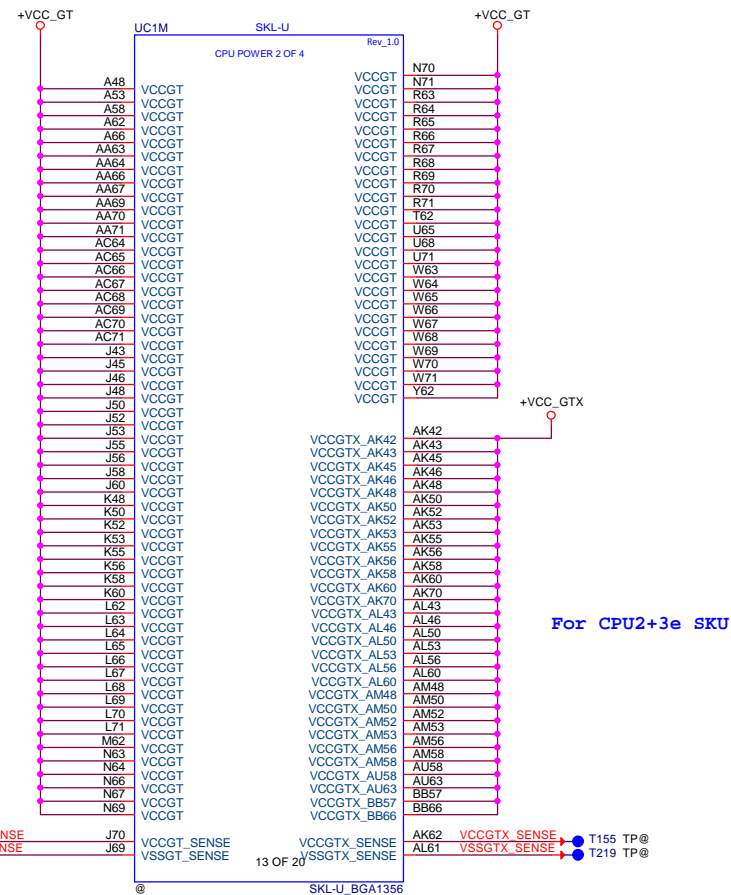
Trace Length < 25 mils

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VSS_SENSE <58>
+1.0VS_VCCSTG

VCCSTG_G20

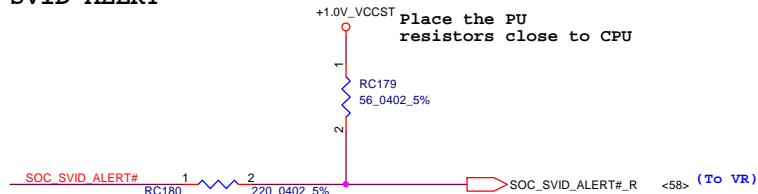
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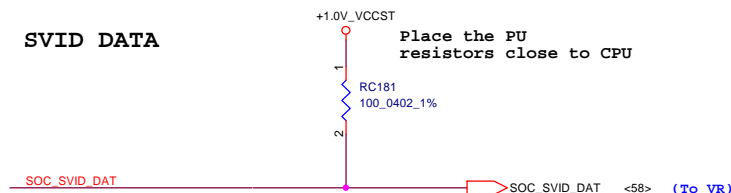


For CPU2+3e SKU

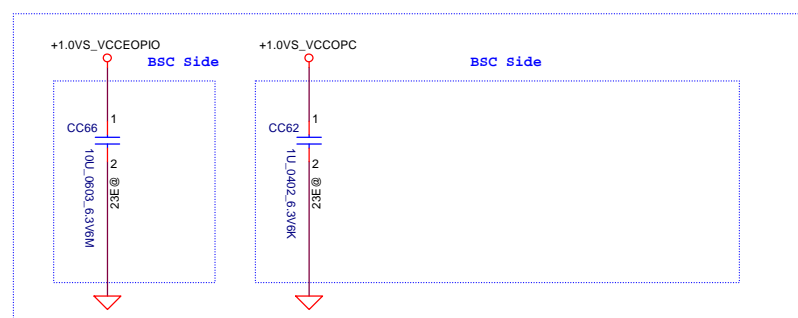
SVID ALERT



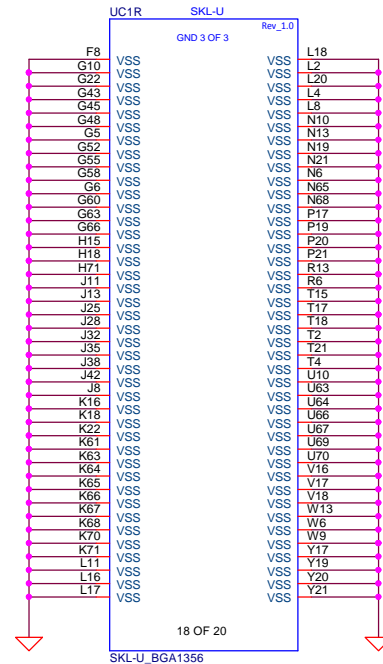
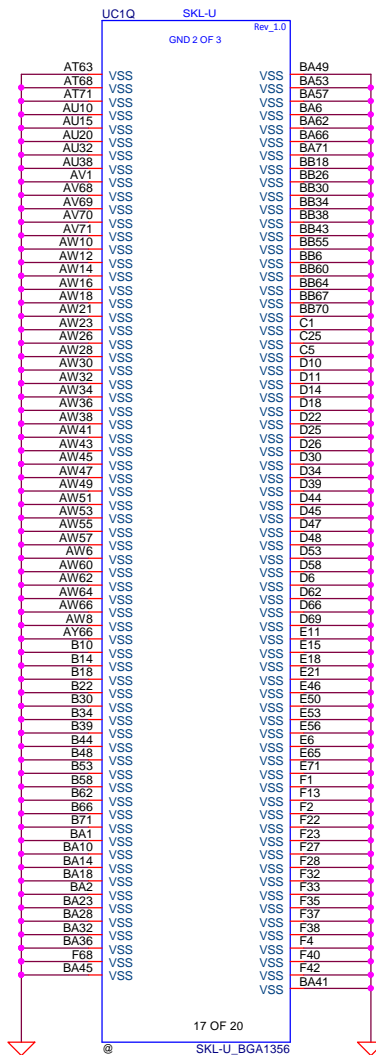
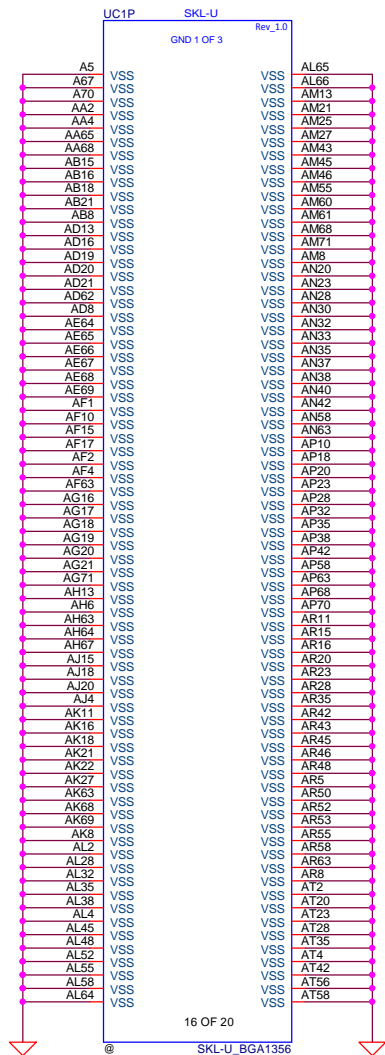
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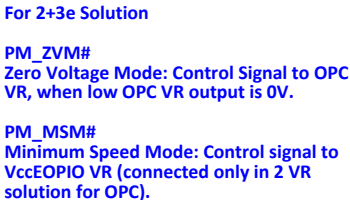
For 2+3e Solution



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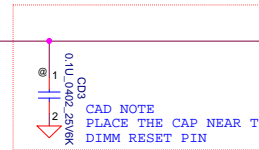
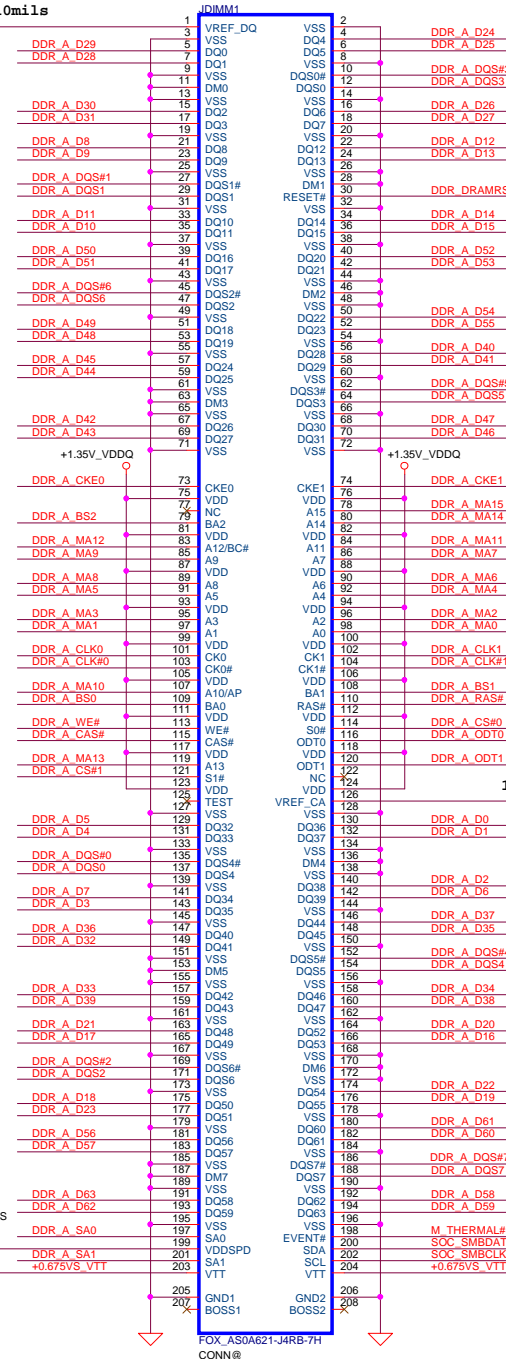
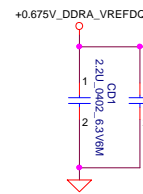
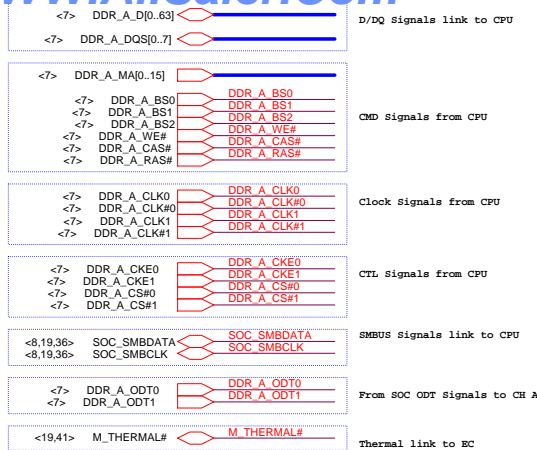


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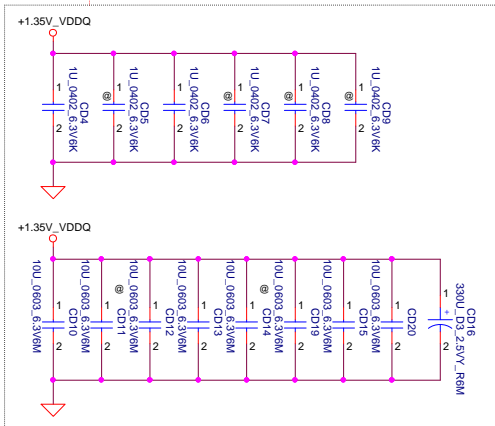
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Reverse Type
2-3A to 1 DIMMs/channel



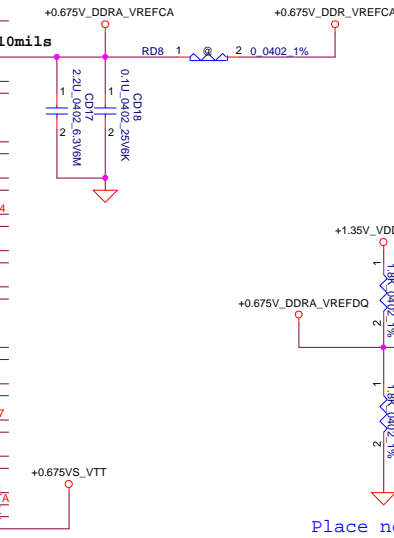
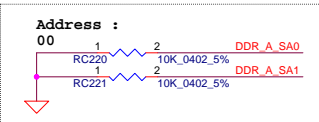
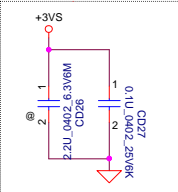
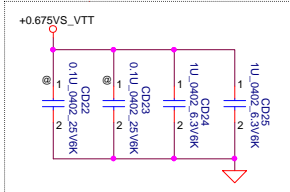
Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket



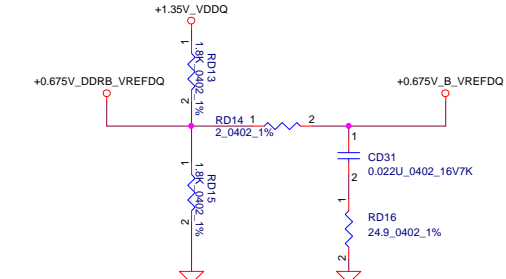
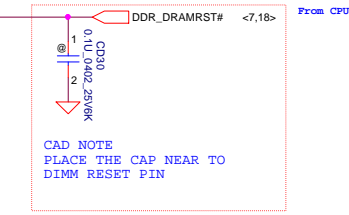
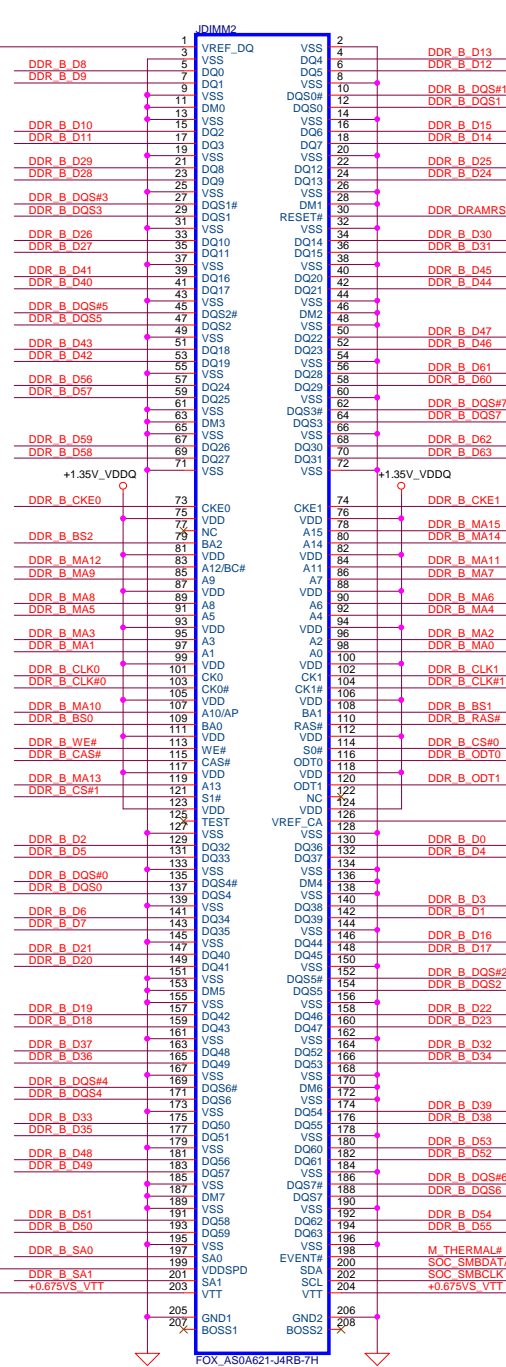
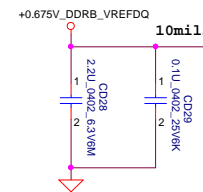
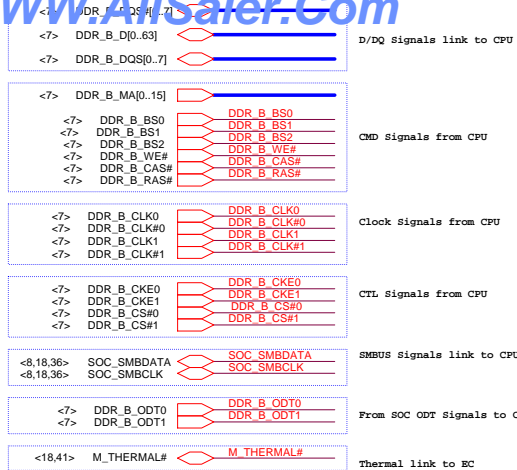
Layout Note:
Place near JDIMM1.203,204

Layout Note:
Place near JDIMM1.199

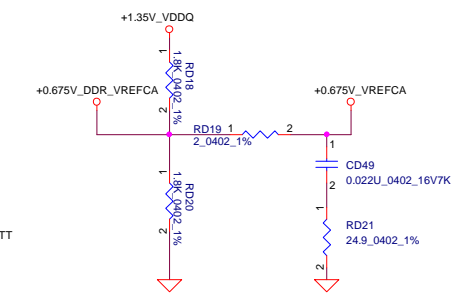
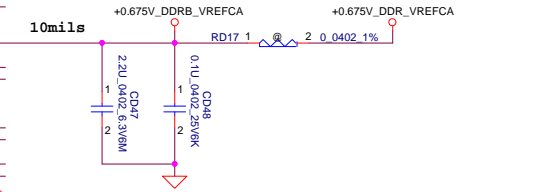


Non- Interleaved Memory

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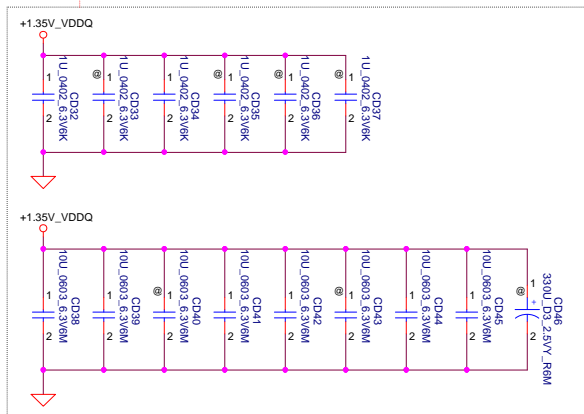
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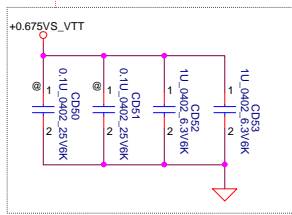
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Non-Interleaved Memory

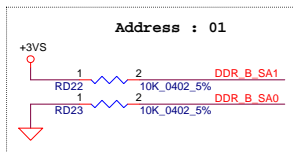
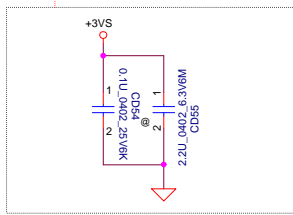
Layout Note:
Place near JDIMM2



Layout Note:
Place near JDIMM2.203,204

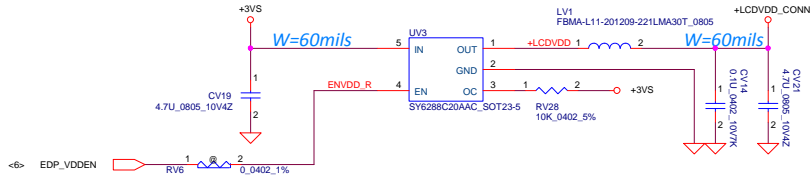


Layout Note:
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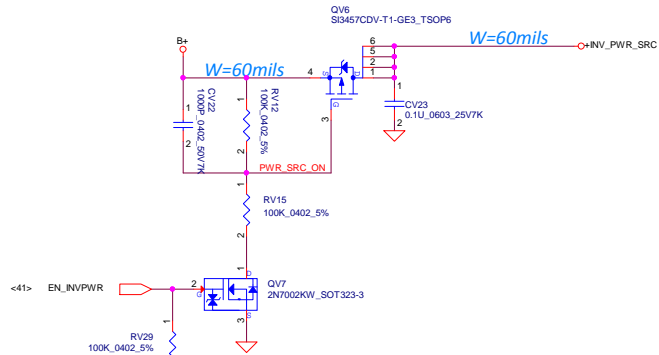


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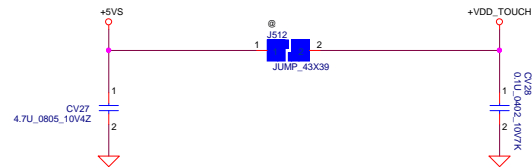
LCD power control



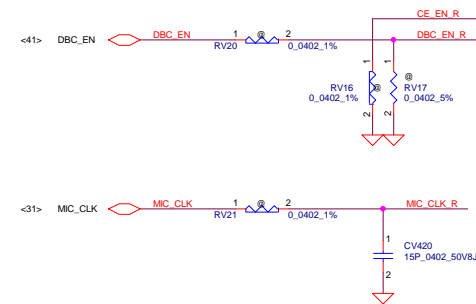
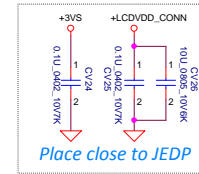
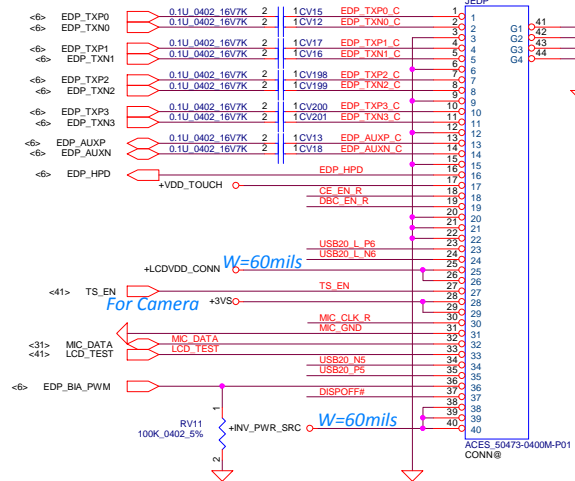
LCD backlight power control

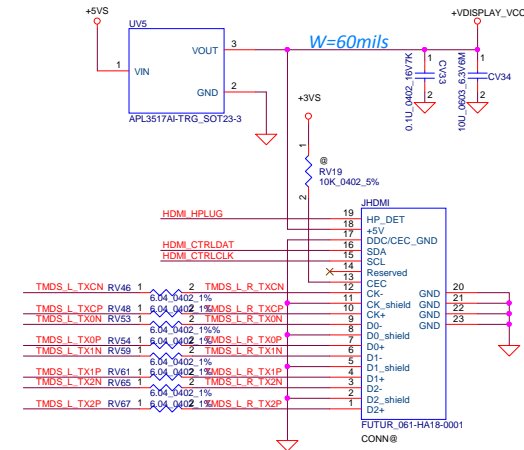
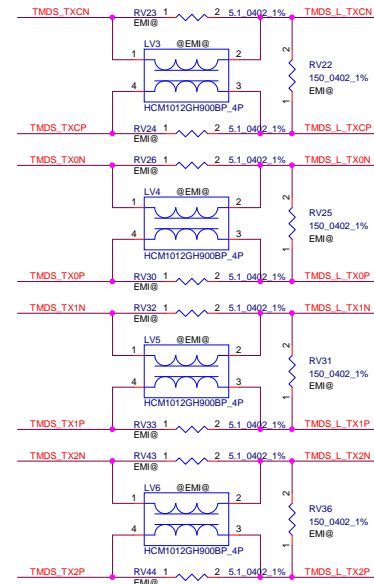
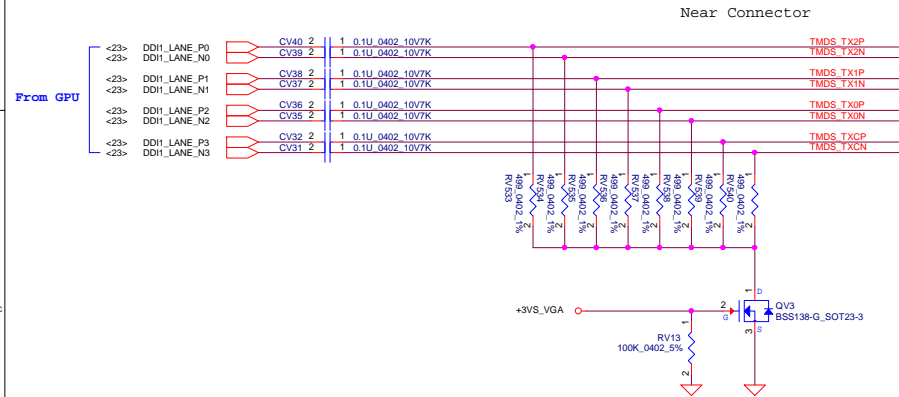


Touch screen panel power control

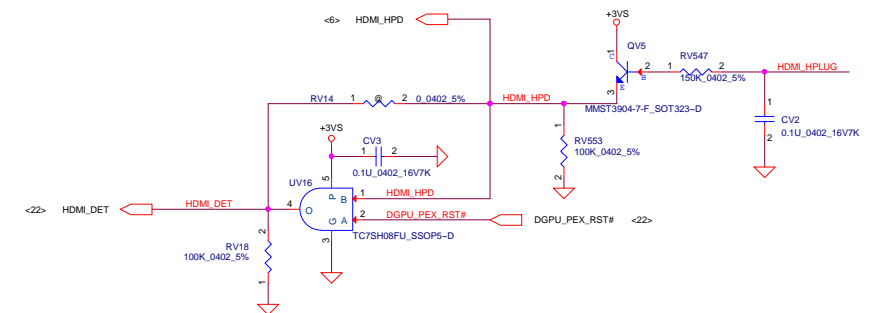
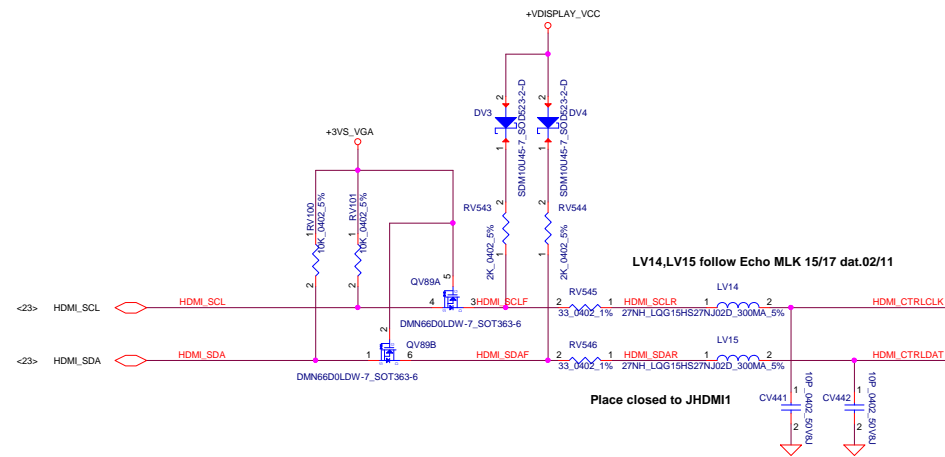


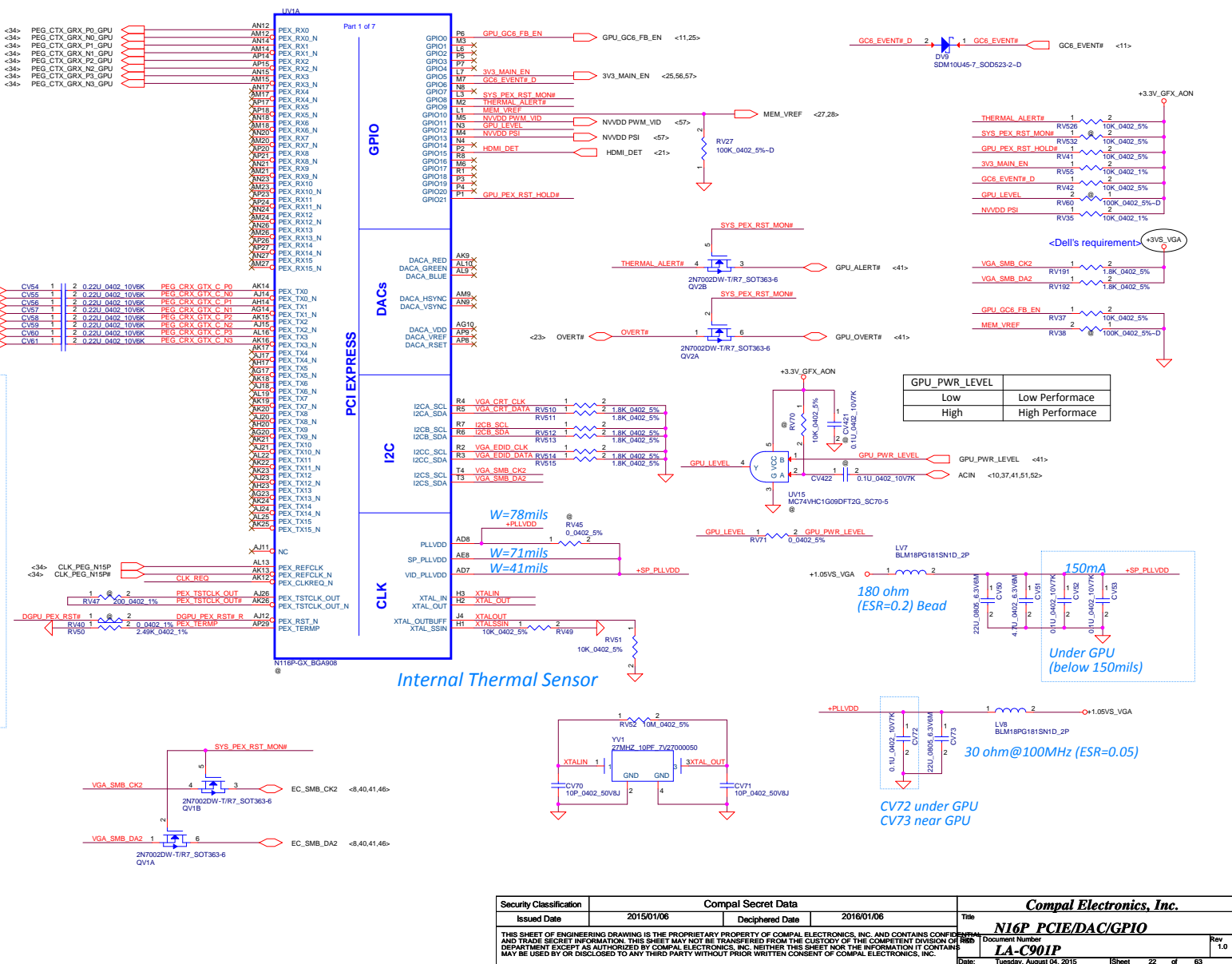
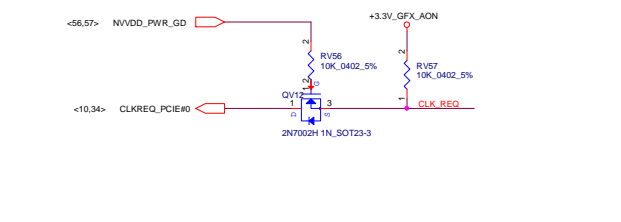
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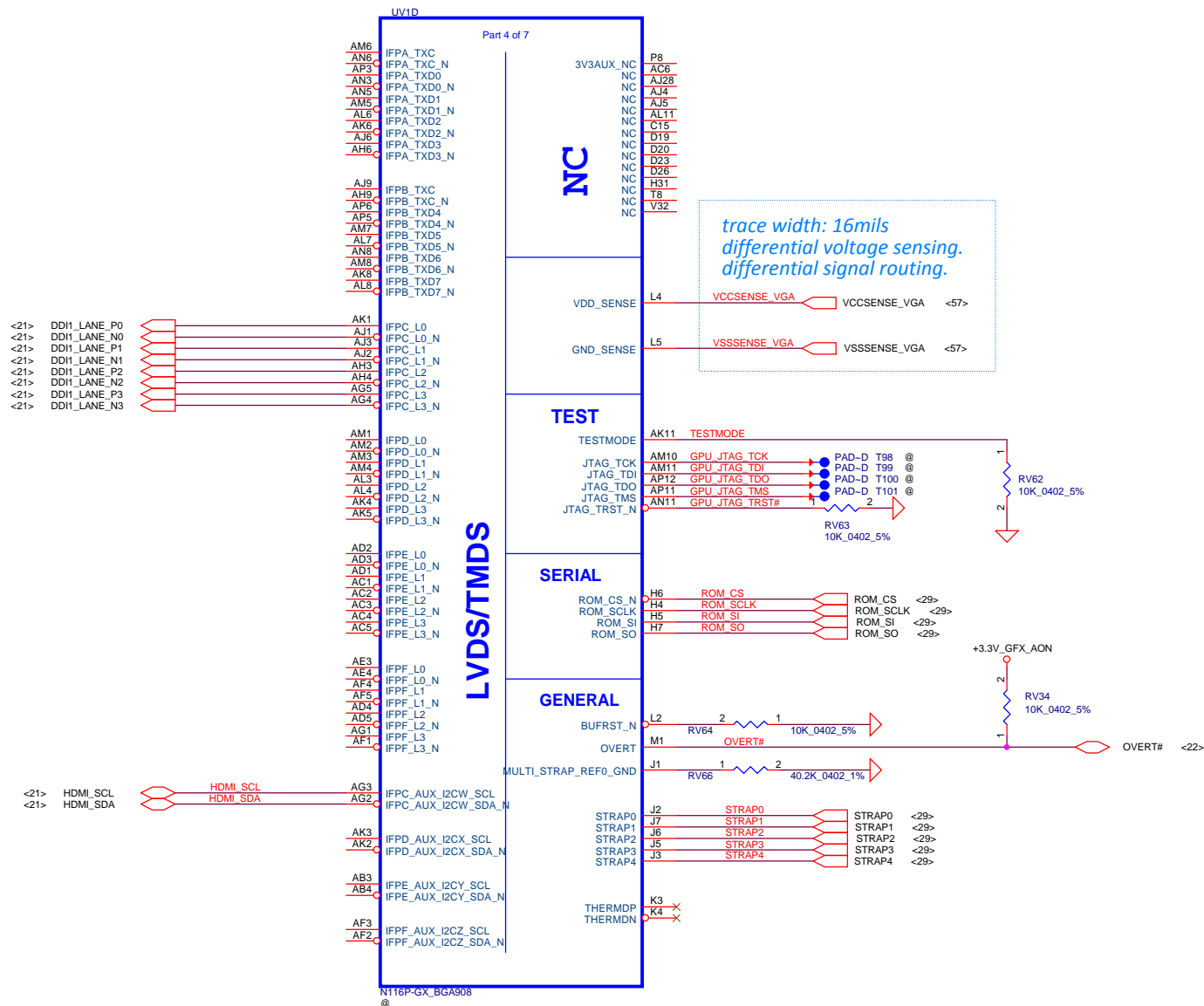




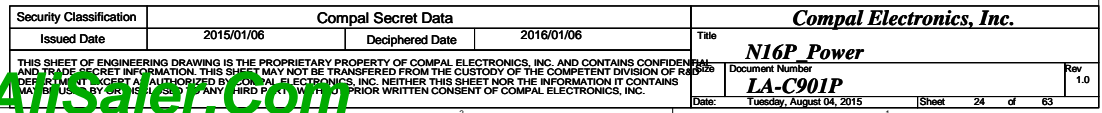
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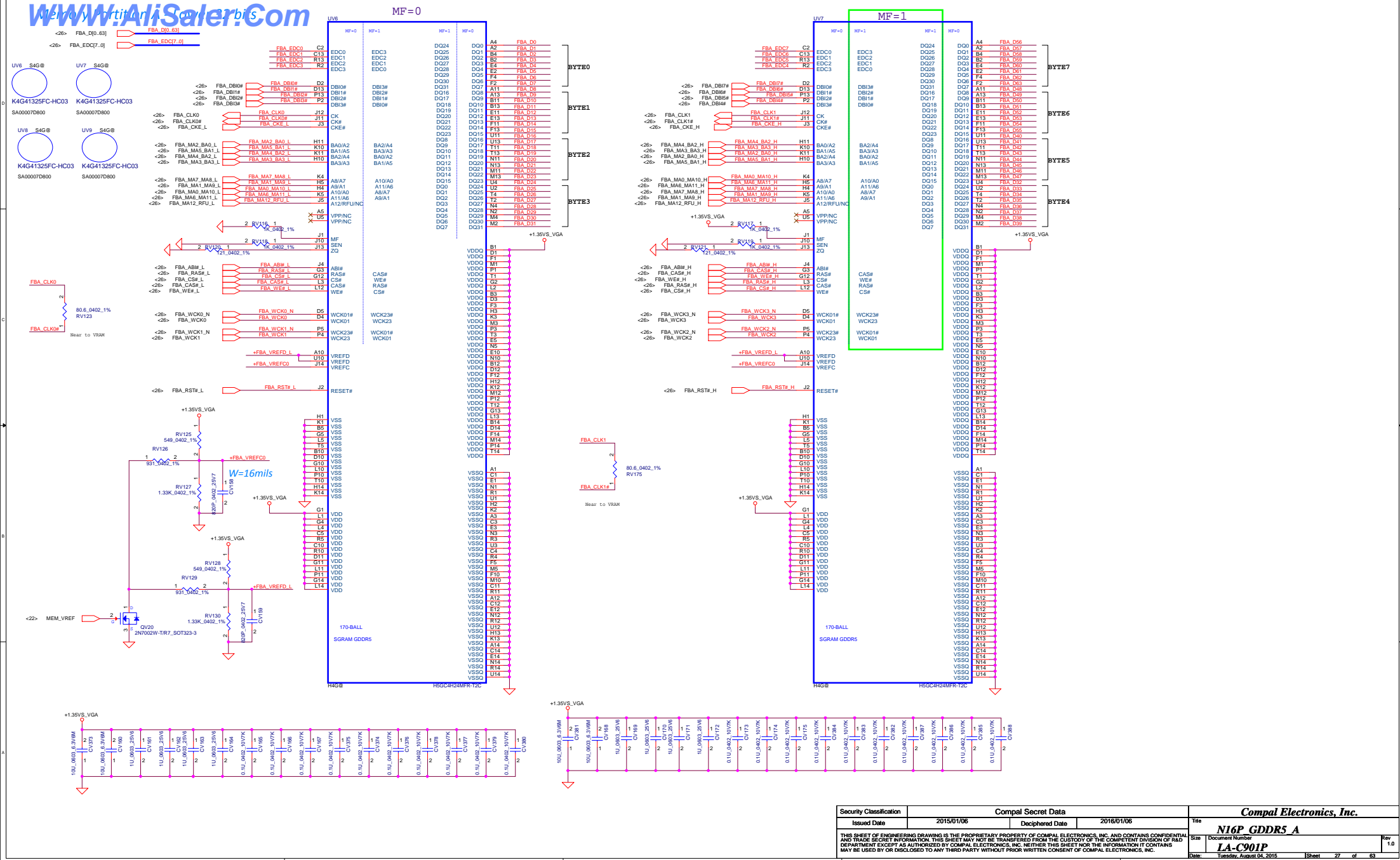


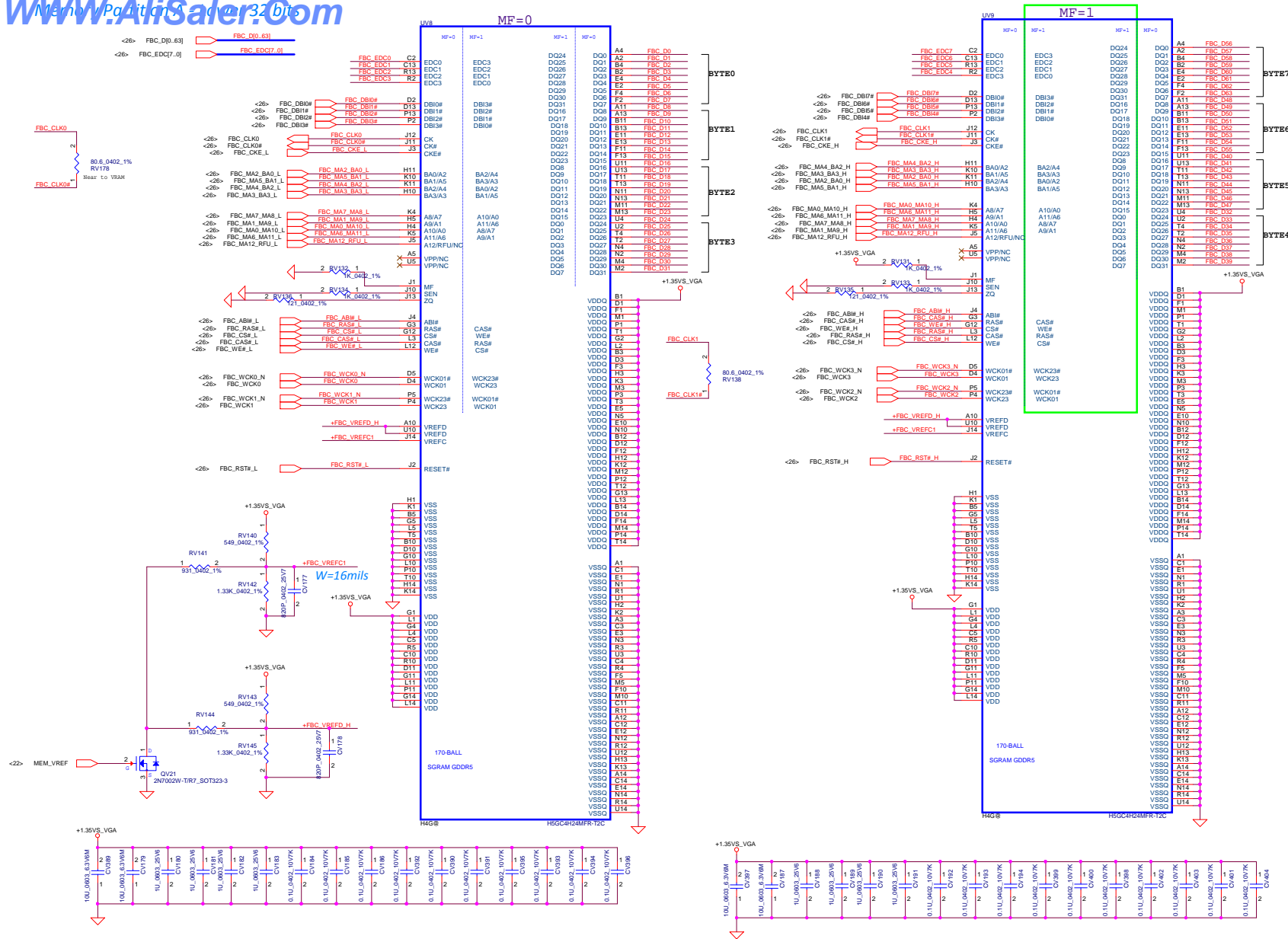


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										LA-C901P	
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										Date	
										Tuesday, August 04, 2015	
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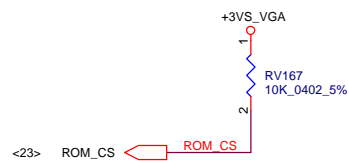
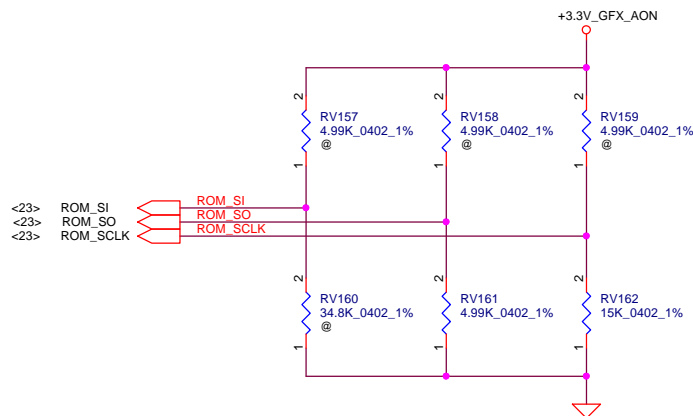




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			Drawing Number LA-C901P	Rev 1.0
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 X7656331L81 : HYNR1@
 X7656331L05 : SAMR3@
 X7656331L09 : HYNR3@

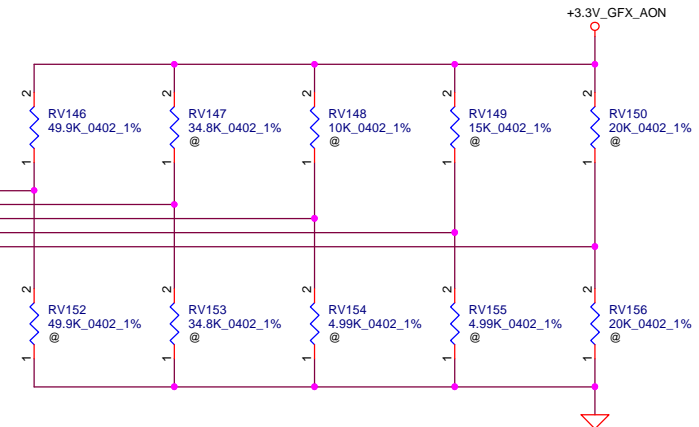
HYNIX 2GB R1
 X7656331L81
 HYNIX 2GB R3
 X7656331L09
 Micron 2GB R3
 X7656331L82



W25X20CL 2M-Bit/256K-byte

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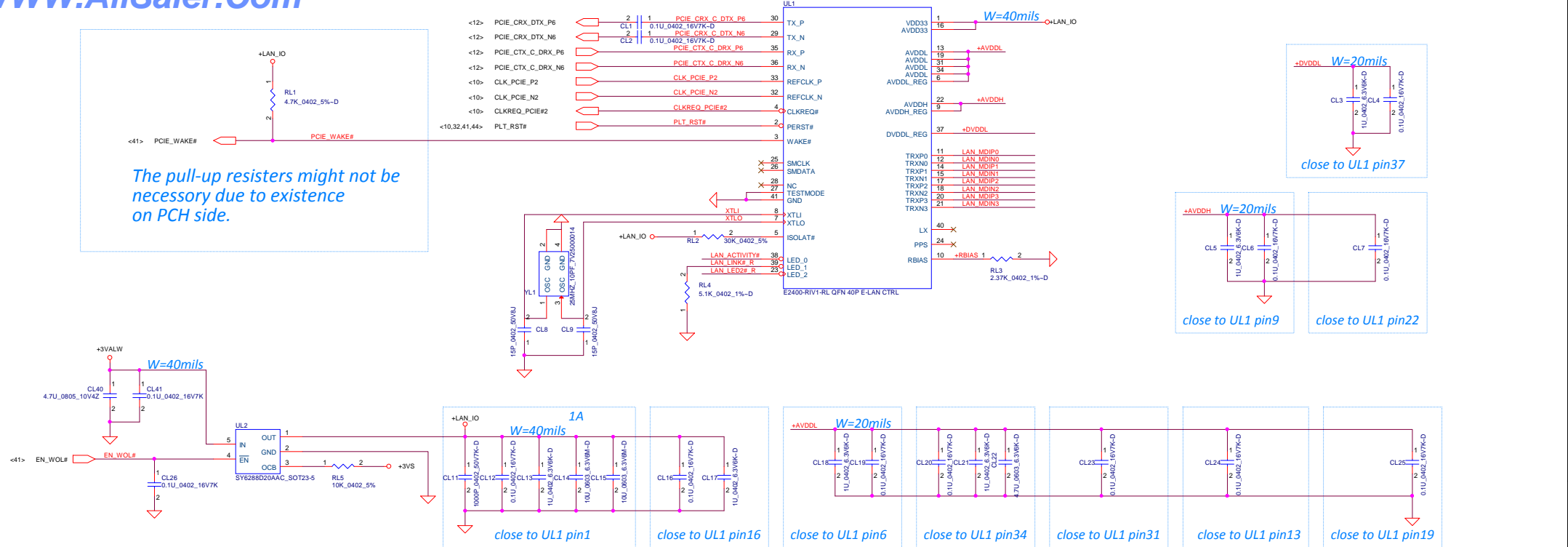
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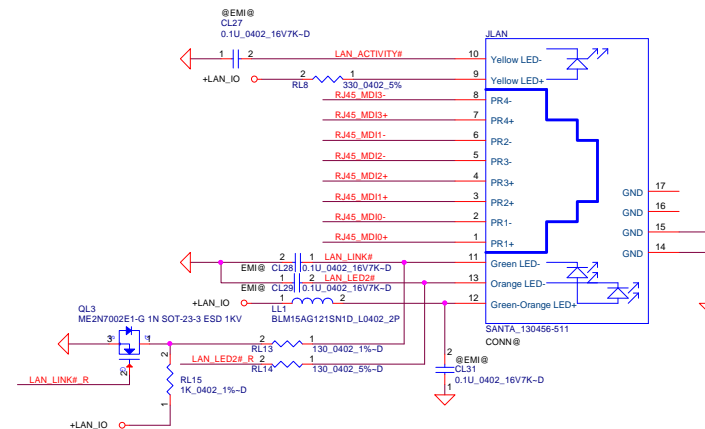
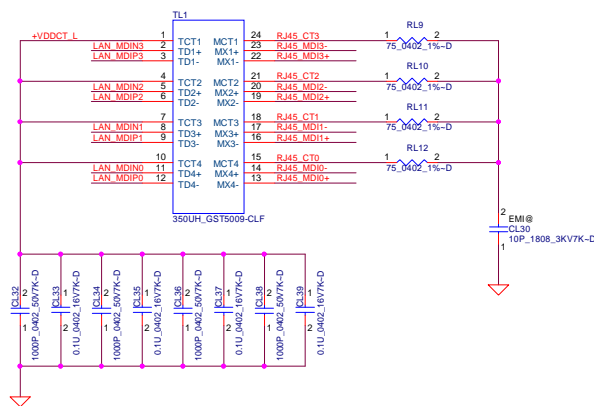
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 SA00008HQ1L S IC D5 128M32/3G H5GC4H24AJR-ROC A31!

GPU	FB Memory GDDR5		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16P-GX	Samsung 2500MHZ	K4G41325FC-HC03	PD 4.99K	PD 4.99K	PD 20K	PU 49.9K	NA	NA	NA	NA
		256Mx16								
	Hynix 2500MHZ	H5GC4H24AJR-R0C	PD 4.99K	PD 4.99K	PD 34.8K	PU 49.9K	NA	NA	NA	NA
		256Mx16								

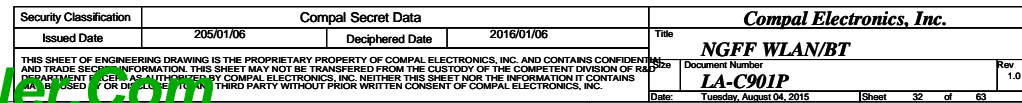
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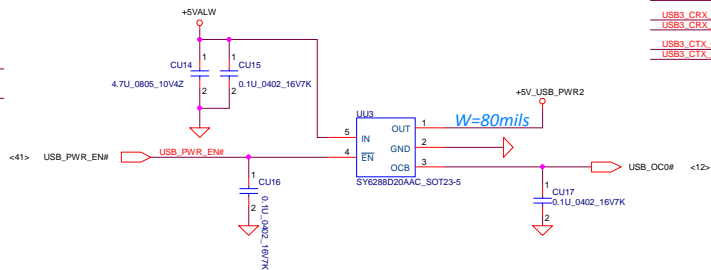
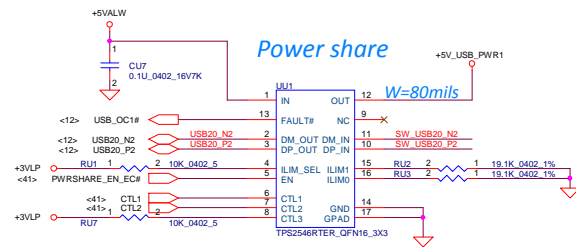
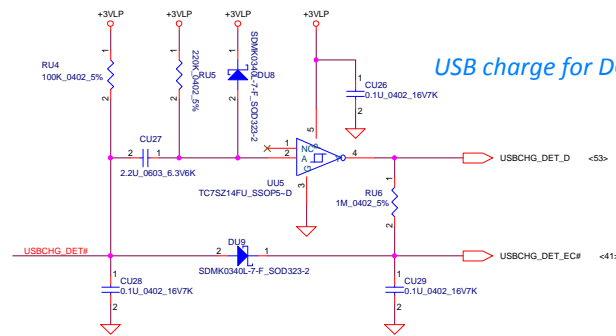
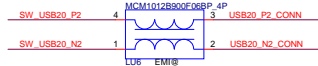
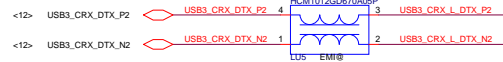
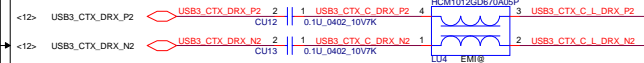
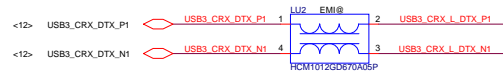


TIMAG: S X'FORM_IH-160 LAN,SP050006F00
BOTH HAND: S X'FORM_GST5009-D LF LAN,SP050006B00

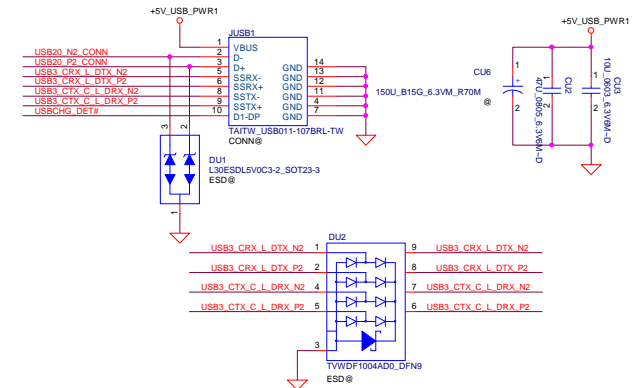


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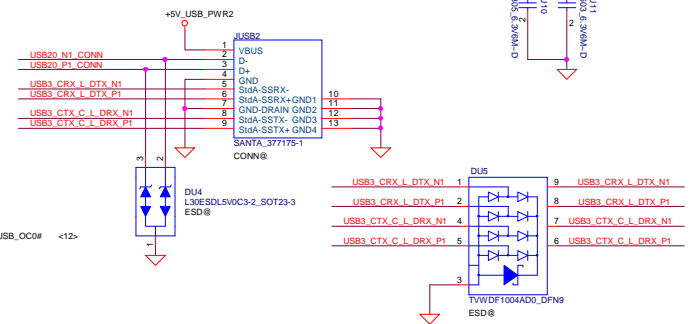




Left side (power share)



Right side



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From CPU RX

Pin Number	HD3SS3415	PI3PCIE3415
21	NC	VDD
25	NC	GND
31	NC	VDD
35	NC	GND
39	NC	VDD

From CPU TX

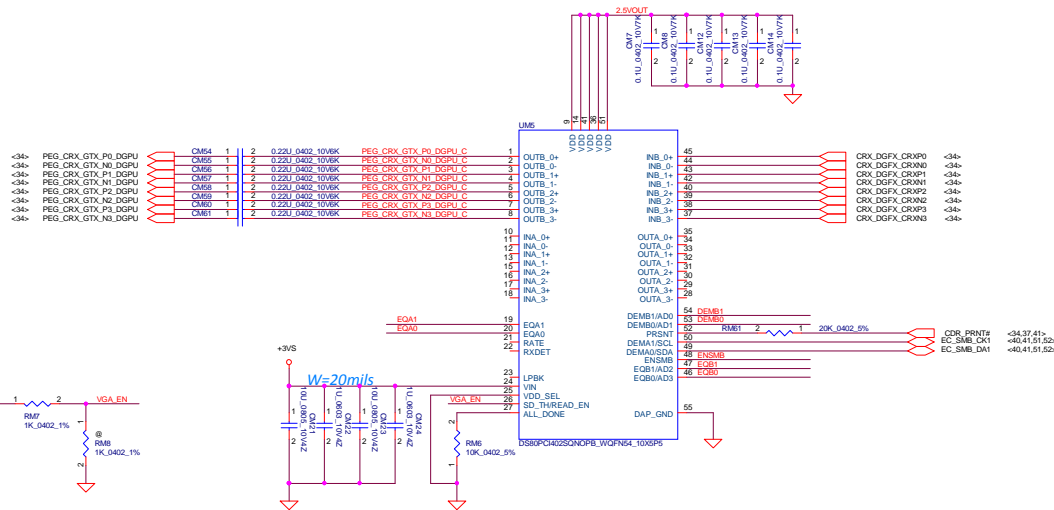
PCIE_CLK_BUFFER

SEL Pin	Function
Low	x1 ----> x0a
High	x1 ----> x0b

To N16P-GX TX

To N16P-GX RX

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Date	2015/01/06	1/Sheet	34 of 63	Rev 1.0



Tie 1KΩ to VDD = Register Access SMBus Slave mode
 FLOAT = Read External EEPROM (Master SMBUS Mode)
 Tie 1KΩ to GND = Pin Mode

EQ Settings

Level	EQA1 EQB1	EOA0 EOB0	dB at 2.5G	dB at 4G	Suggested Use
1	0	0	3.7	4.9	< 5 inch trace
2	0	R	5.8	7.9	5 inch 5-mil trace
3	0	F	7.7	9.9	5 inch 4-mil trace
4	R	1	8.9	11	10 inch 5-mil trace
5	R	0	11.2	14.3	10 inch 4-mil trace
6	R	R	11.4	14.6	15 inch 4-mil trace
7	R	F	13.5	17	20 inch 4-mil trace
8	R	1	15	18.5	25 to 30 inch 4-mil trace
9	F	0	12.8	18	30 inch 4-mil trace
10	F	R	17.4	22	35 inch 4-mil trace
11	F	F	19.7	24.4	10m, 30awg cable
12	F	1	21.1	25.8	
13	1	0	21.7	27.4	
14	1	R	23.5	29.0	10m - 12m cable
15	1	F	25.8	31.4	
16	1	1	27.3	32.7	

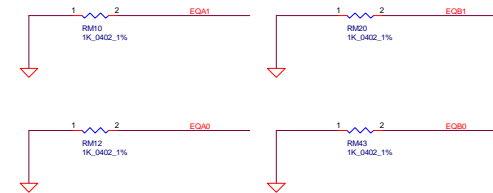
DEMA Settings

Level	DEMA1 DEMB1	DEMA0 DEMB0	DEM dB	Suggested Use
1	0	0	0	< 5 inch 4-mil trace
2	0	R	0	< 5 inch 4-mil trace
3	0	F	-3.5	10 inch 4-mil trace
4	0	1	0	< 5 inch 4-mil trace
5	R	0	-3.5	10 inch 4-mil trace
6	R	R	-6	15 inch 4-mil trace
7	R	F	0	< 5 inch 4-mil trace
8	R	1	-3.5	10 inch 4-mil trace
9	F	0	-6	15 inch 4-mil trace
10	F	R	0	< 5 inch 4-mil trace
11	F	F	-3.5	10 inch 4-mil trace
12	F	1	-6	15 inch 4-mil trace
13	1	0	0	< 5 inch 4-mil trace
14	1	R	-3.5	10 inch 4-mil trace
15	1	F	-6	15 inch 4-mil trace
16	1	1	-9	20 inch 4-mil trace

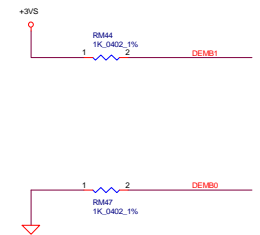
Level control Settings

Level	Pin Setting	Description	Suggested Use
1	0	1kΩ to GND	< 5 inch 4-mil trace
2	R	20kΩ to GND	< 5 inch 4-mil trace
3	F	Float	10 inch 4-mil trace
4	1	1kΩ to VDD	< 5 inch 4-mil trace

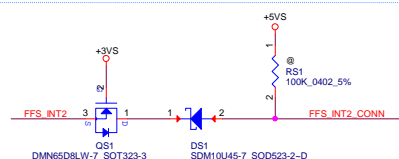
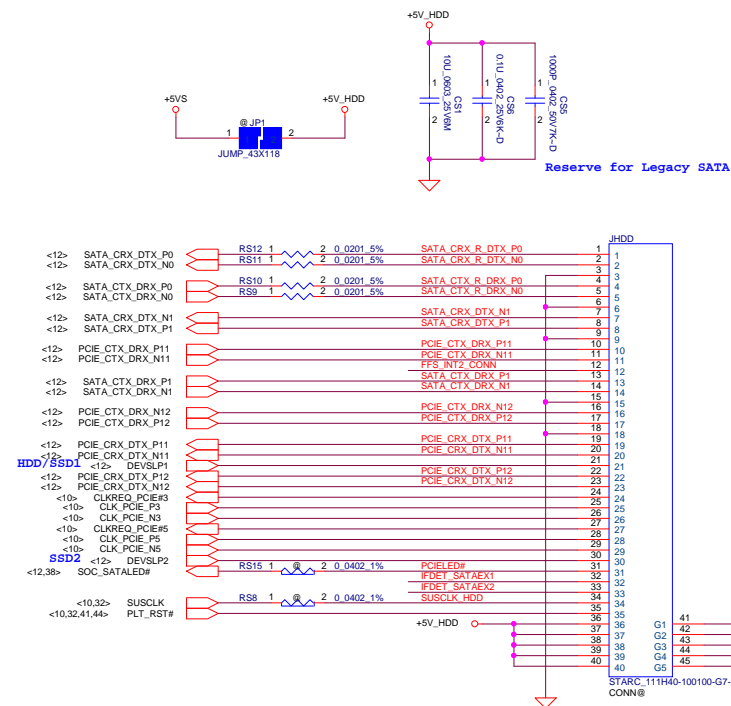
EQ*MB



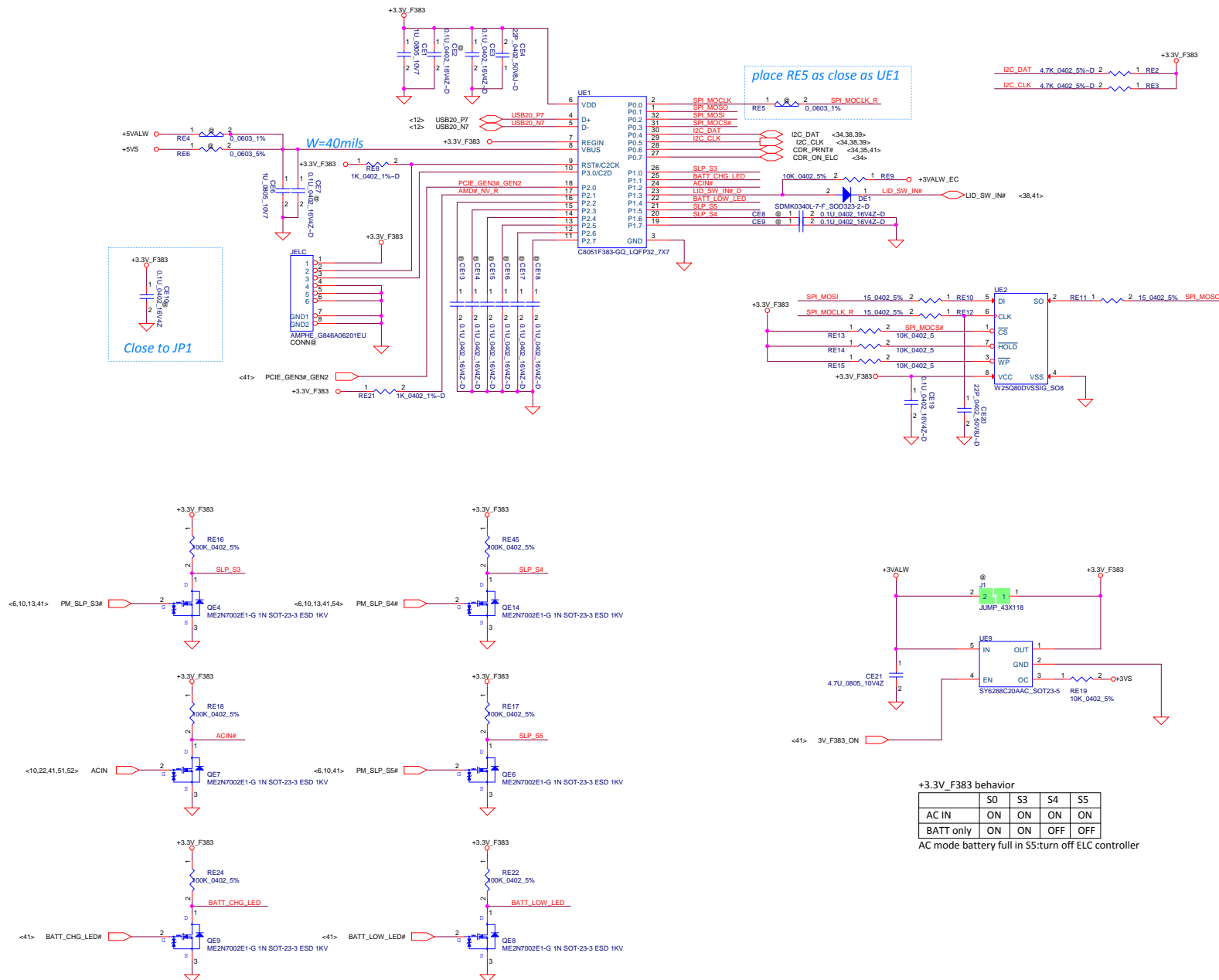
DEM*EGPU

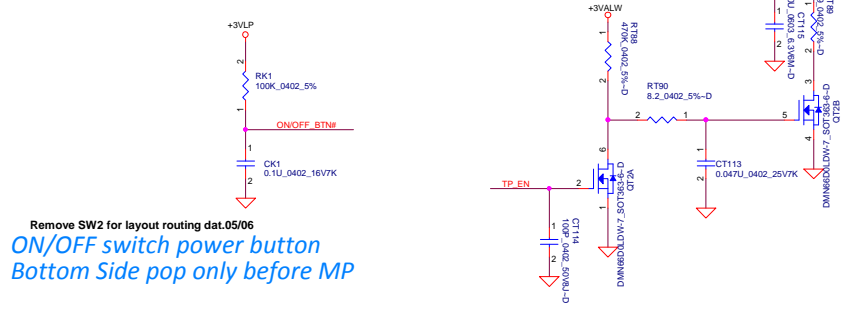
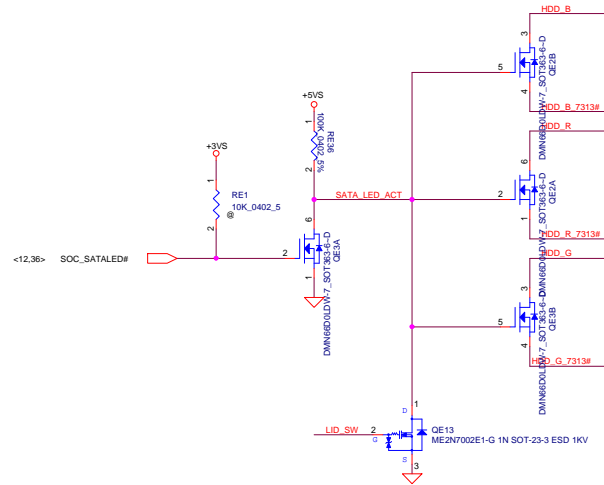
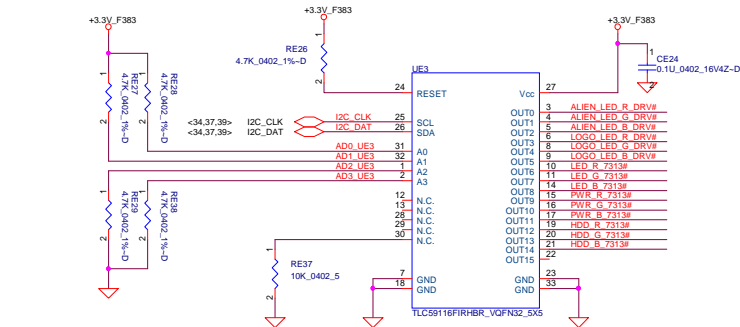


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LA-C901P				Rev. 1.0
Date: January 03, 2015				Sheet 35 of 63



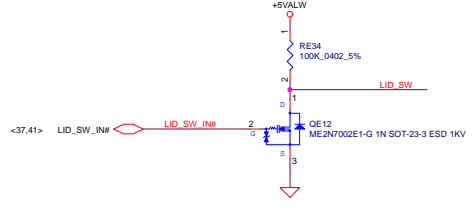
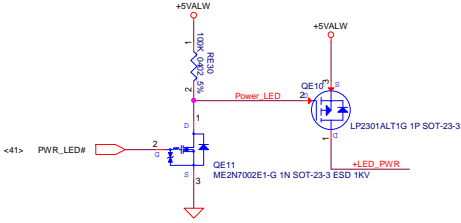
DET_SATA#/PCI-E	Module Type
0	SATA
1	PCI-E



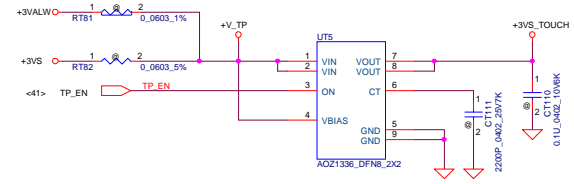


Remove SW2 for layout routing dat.05/06
ON/OFF switch power button
Bottom Side pop only before MP

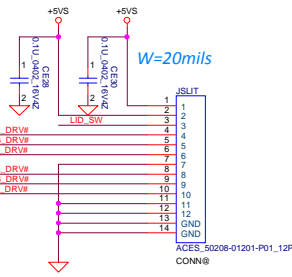
Power LED



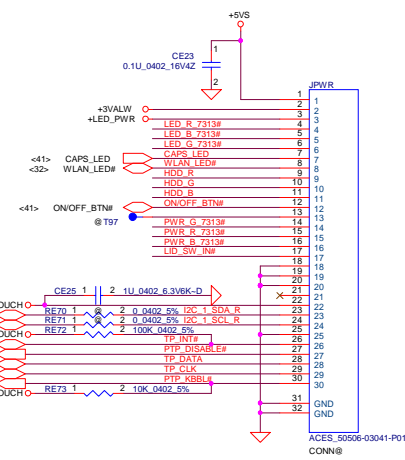
PTP pin define
VDD
I2C_DATA
I2C_CLK
GND
ATTN
PTP_DISABLE#(CLOSE LID)
PS2_DATA
PS2_CLK
PTP_KBBL#(KB BL)
NC



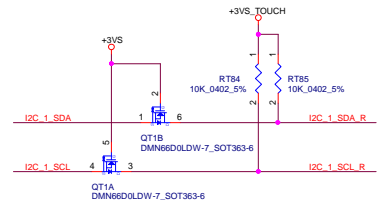
AOZ1336(SA00006U600)
TPS22967(SA000070S00)



Logic up LED board



Logic low LED board

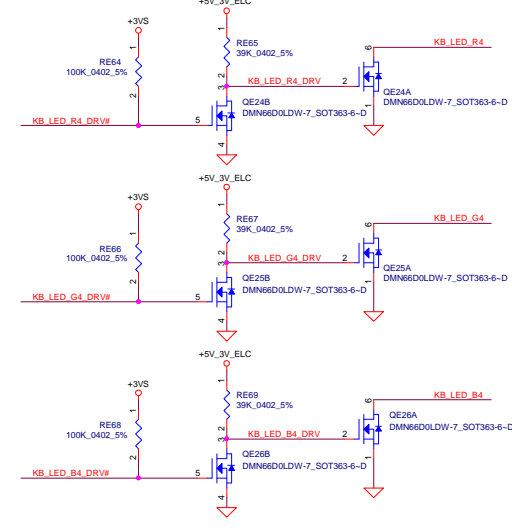
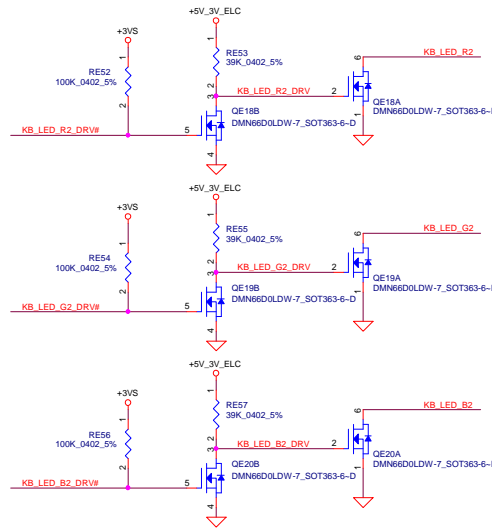
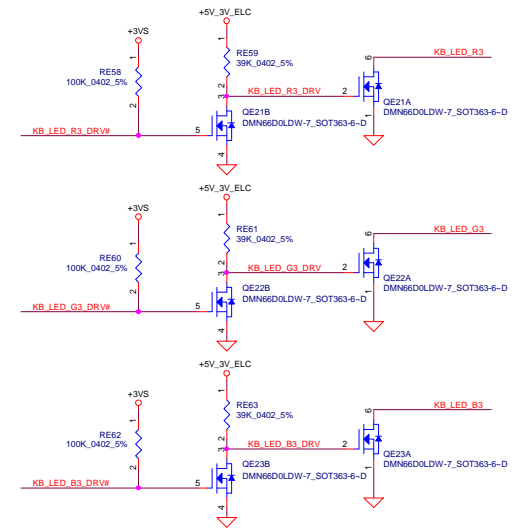
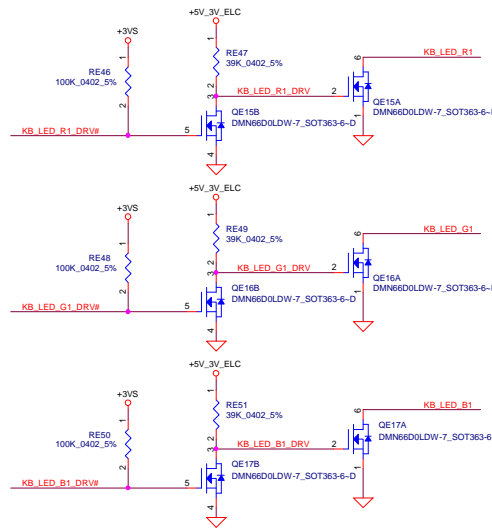
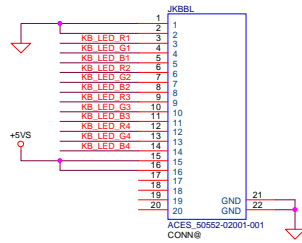
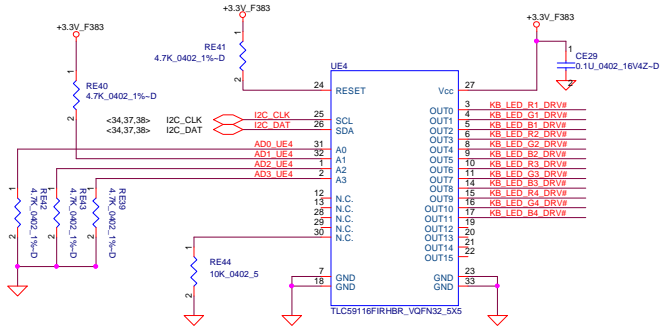
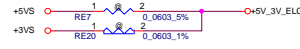


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Document Number				Rev
LA-C901P				1.0
Date: Tuesday, August 04, 2015				Sheet 38 of 63

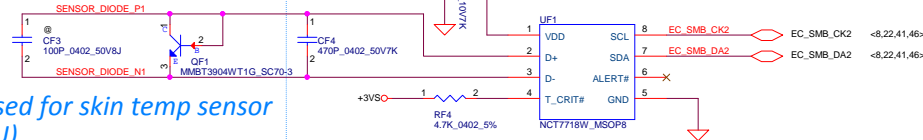
I2C address

	A3	A2	A1	A0
UE1 (sheet 10 in Caldera board)	0	0	0	1
UE4 (sheet 39)	0	0	1	0
UE3 (sheet 38)	0	0	1	1
3rd LED drive (reserve)	0	1	0	0

Default use +3VS

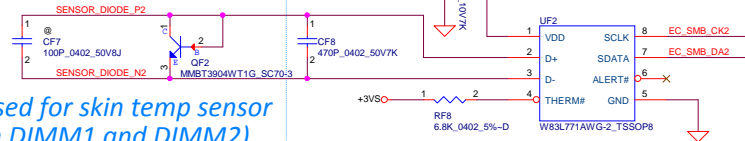


Main:
NCT7718W(SA000067P00)
Address:1001_100xb(0x98)
Second:
ADM1032ARMZ-REEL(SA010320110)
Address:100_1100(0x4C)

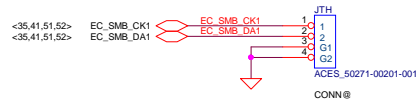


Diode circuit s used for skin temp sensor
(placed near CPU).
Place CF3 close to QF1 as possible.

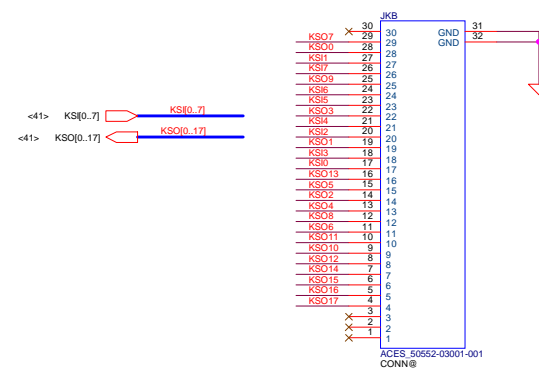
Main:
W83L771AWG-2(SA00003PU00)
Address:1001_101xb(0x9A)
Second:
ADM1032ARMZ-2R(SA010320120)
Address:100_1101(0x4D)



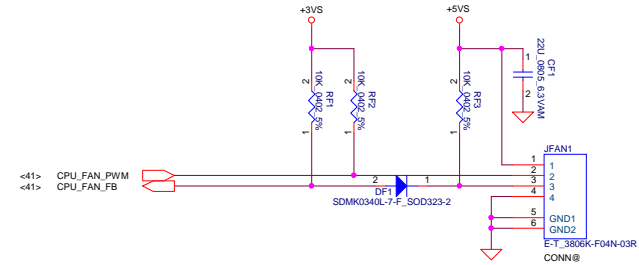
Diode circuit s used for skin temp sensor
(placed between DIMM1 and DIMM2).
Place CF7 close to QF2 as possible.



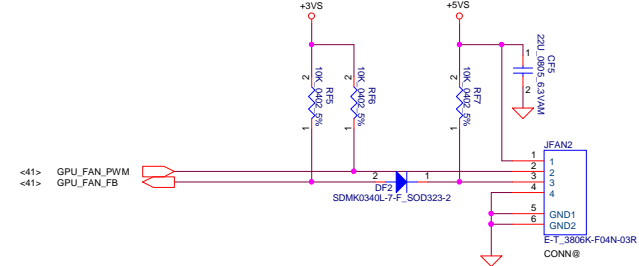
INT_KBD Connector

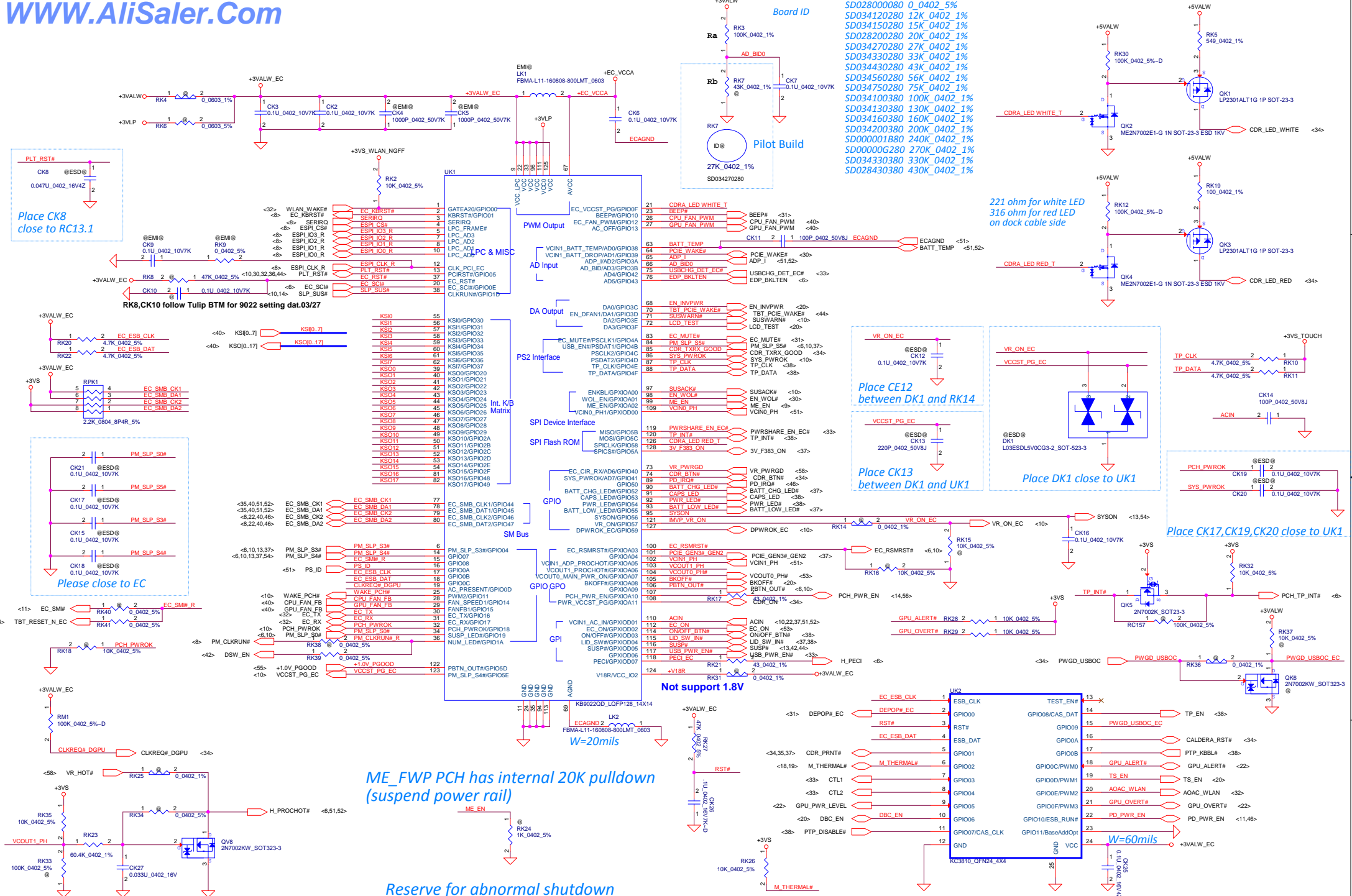


CPU FAN control circuit

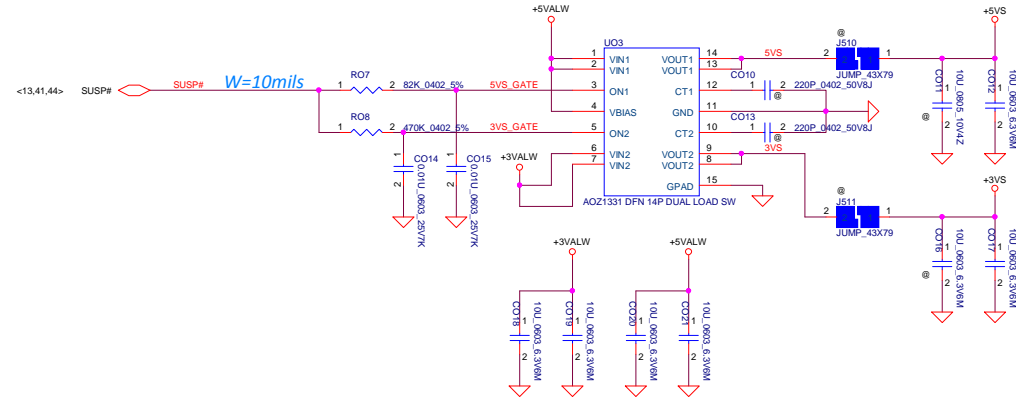


GPU FAN control circuit

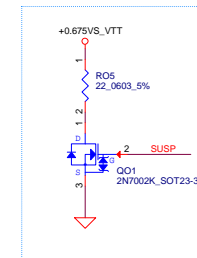
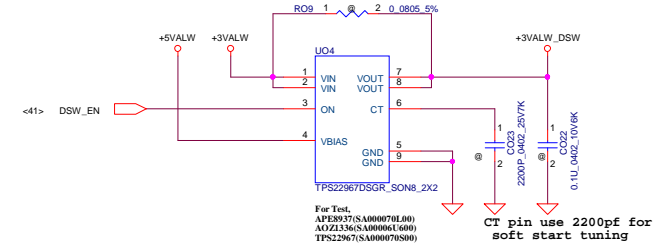




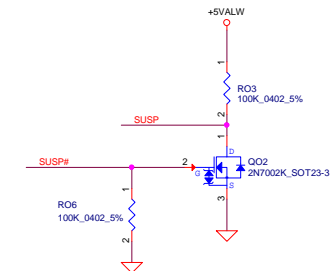
+5VS and +3VS switch



+3VALW TO +3VALW_DSW



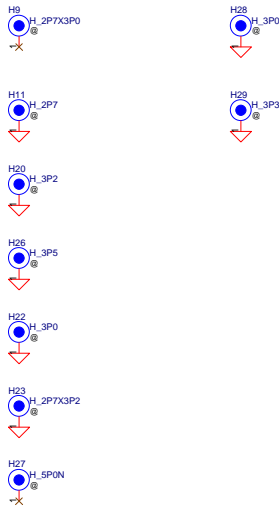
For Intel S3 power reduction



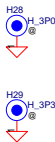
Screw Hole



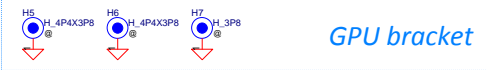
Echo MLK delete H24,H25



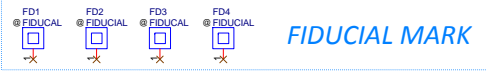
Add H28,H29 for USB3.1 type C



CPU bracket



GPU bracket



FIDUCIAL MARK

S IC DSL6340 SLKYB B0 FC-CSP I/O CONTROL

SA000090N0L

ARES2R1@



S IC A31 DSL6340 QSCX B0 THUNDERBOLT

SA000090N0L

ARGSR3@

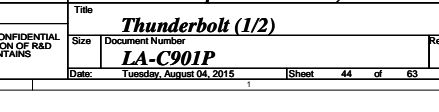
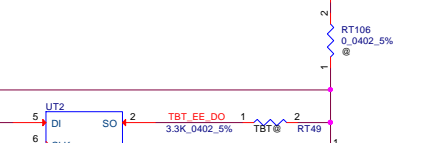
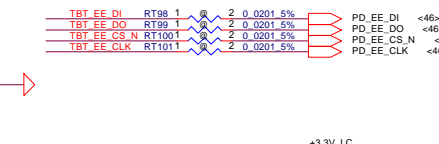
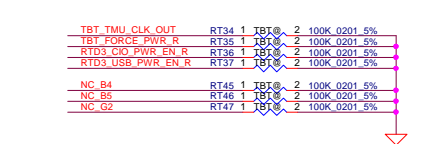
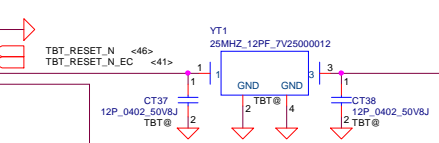
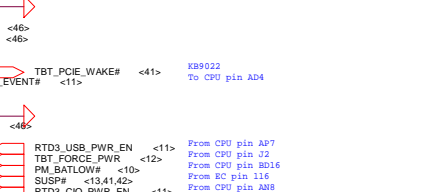
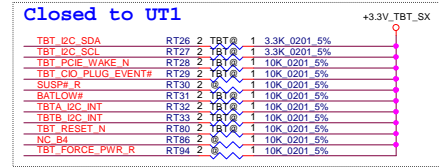
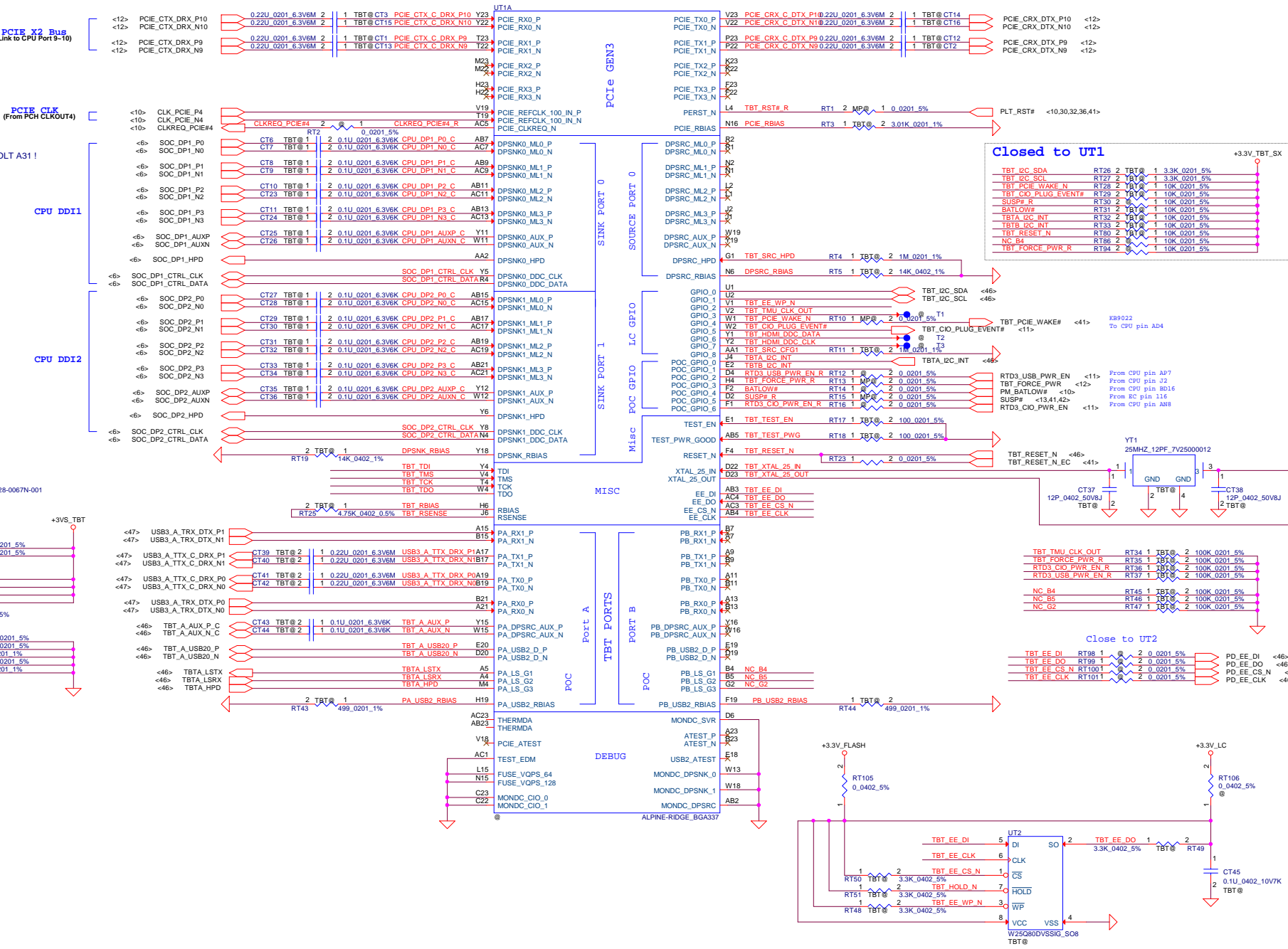
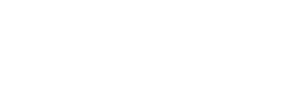
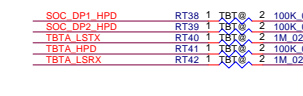
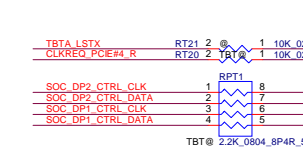
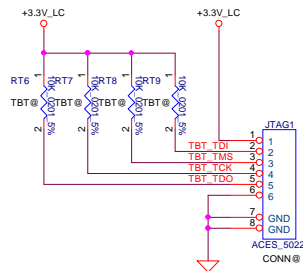
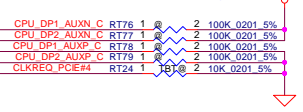


S IC DSL6340 SLL42 B1 FCCSP 337P THUNDERBOLT A31 !

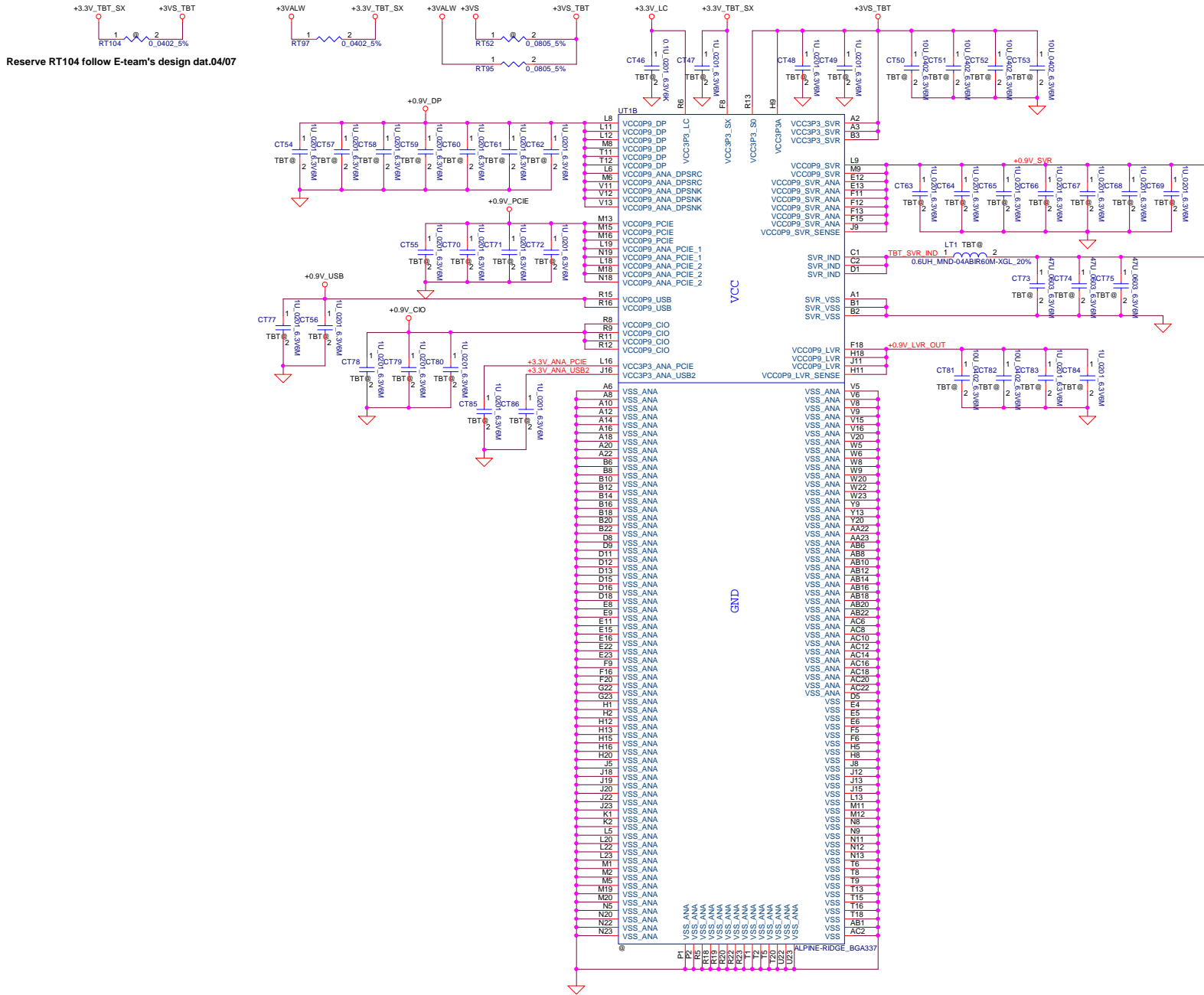
SA000090N0L

ARGSR3@

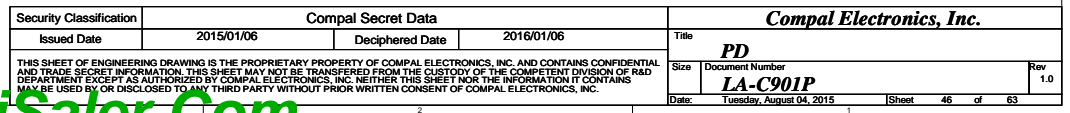
Reserve for common DP design

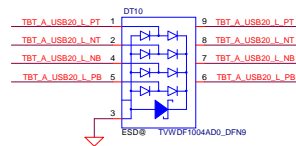
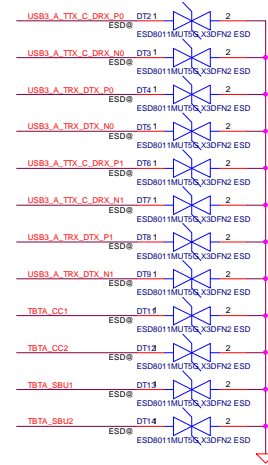
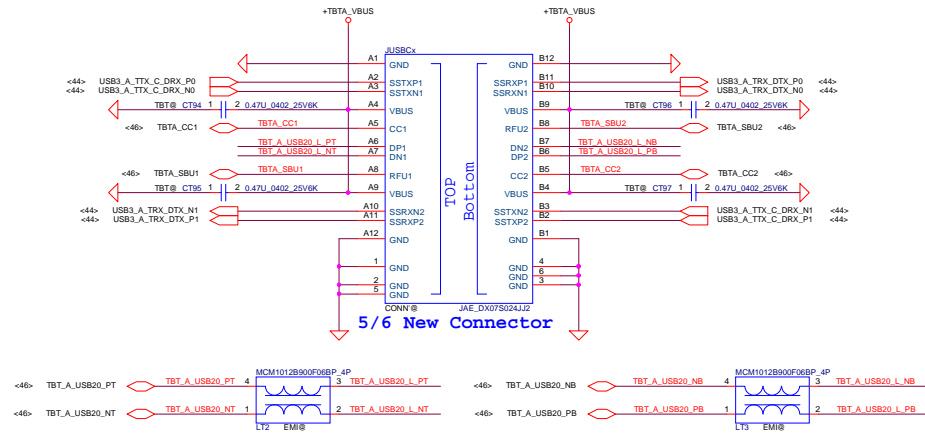


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Date: Tuesday, August 04, 2015				Sheet 44 of 63



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				Sheet	45 of 63
				Rev	1.0
				LA-C901P	

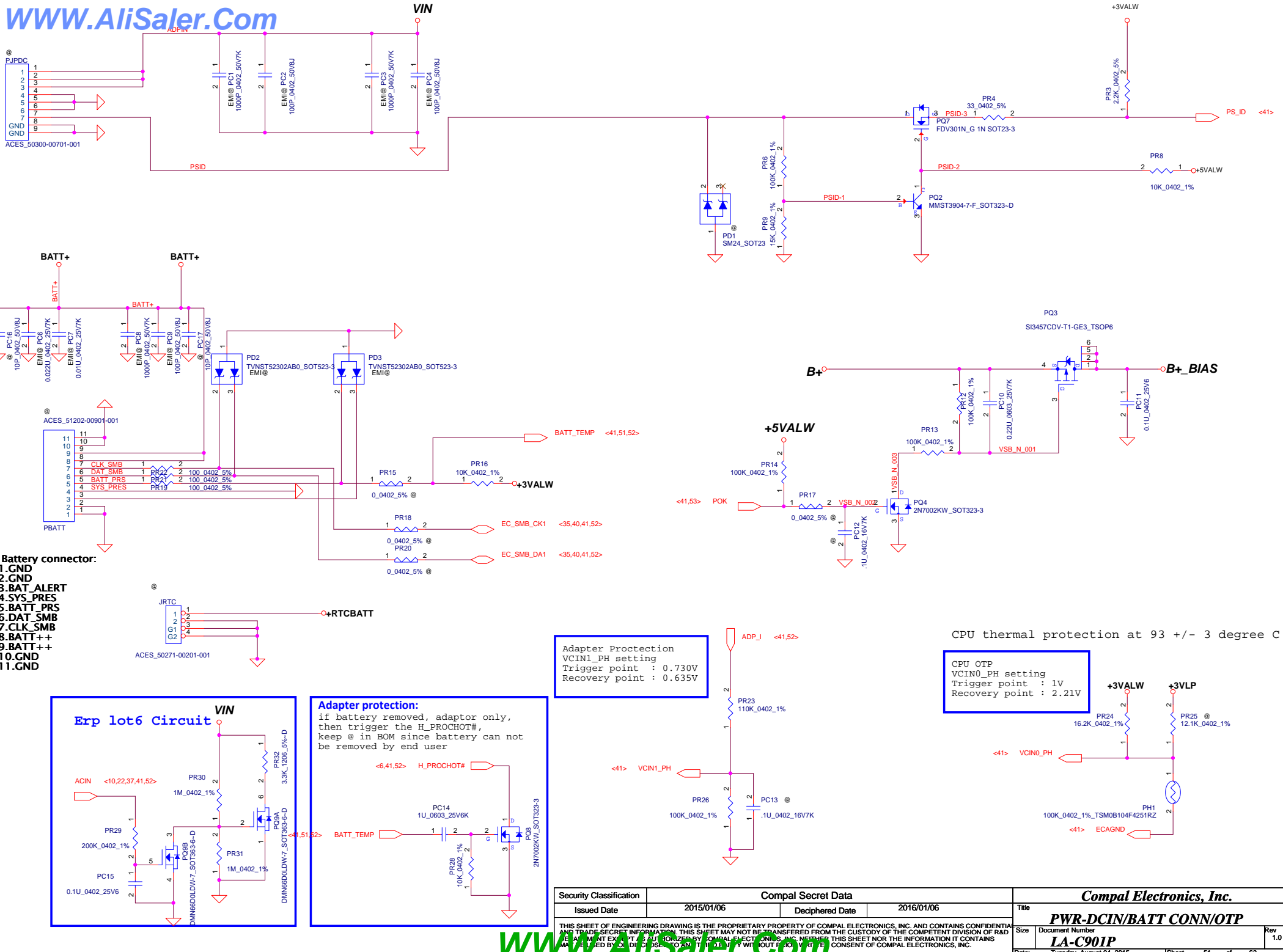




Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1				HW			
2				HW			
3				HW			
4				HW			
5				HW			
6				HW			
7				HW			
8				HW			
9				HW			
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42				HW			

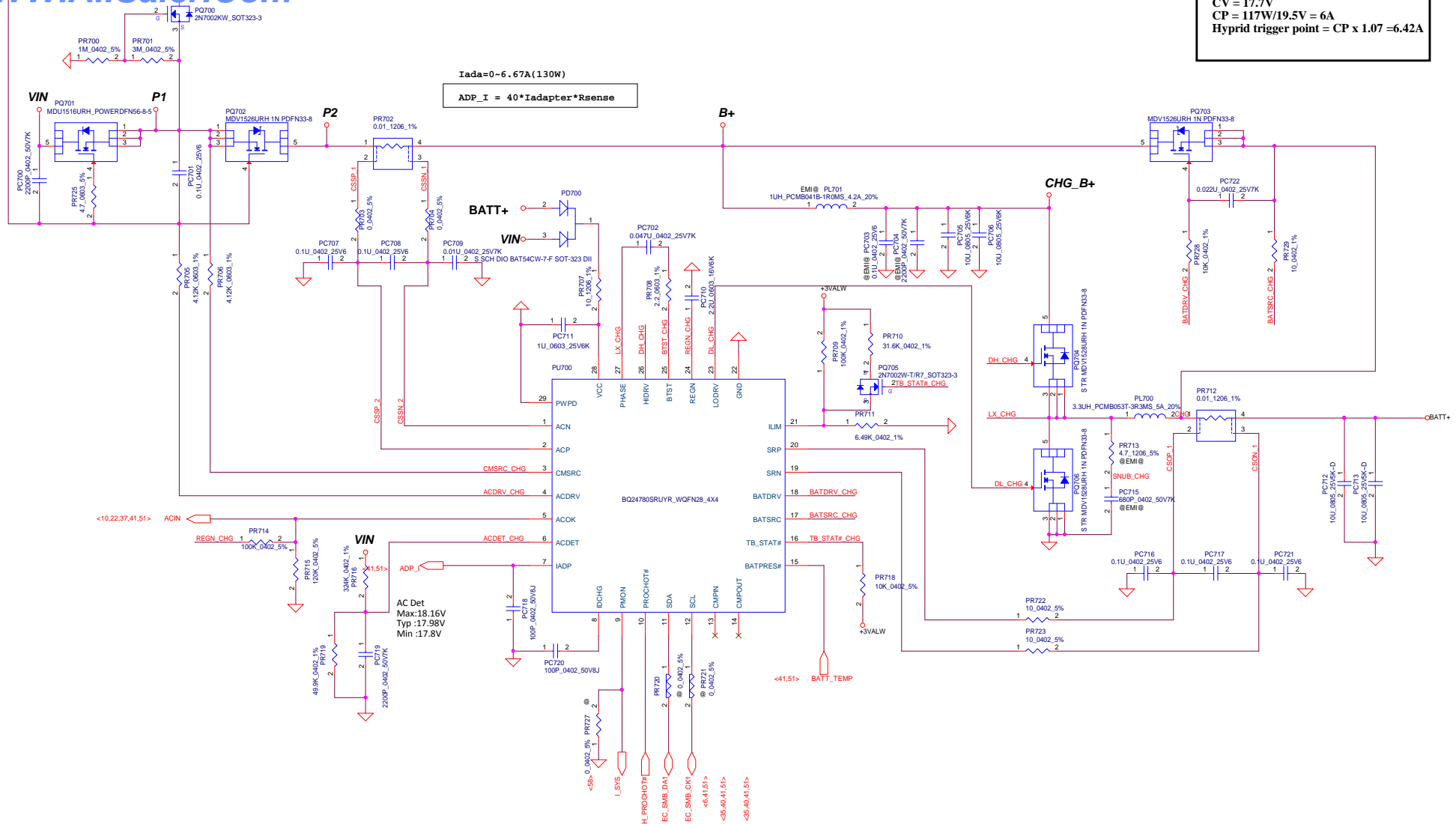
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44				HW			
45				HW			
46				HW			
47				HW			
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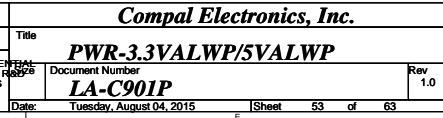
Security Classification		Compal Secret Data		<div>Compal Electronics, Inc.</div>	
Issued Date	2015/01/06	Deciphered Date	2016/01/06	Title	<div>HW-PIR Page.3</div>
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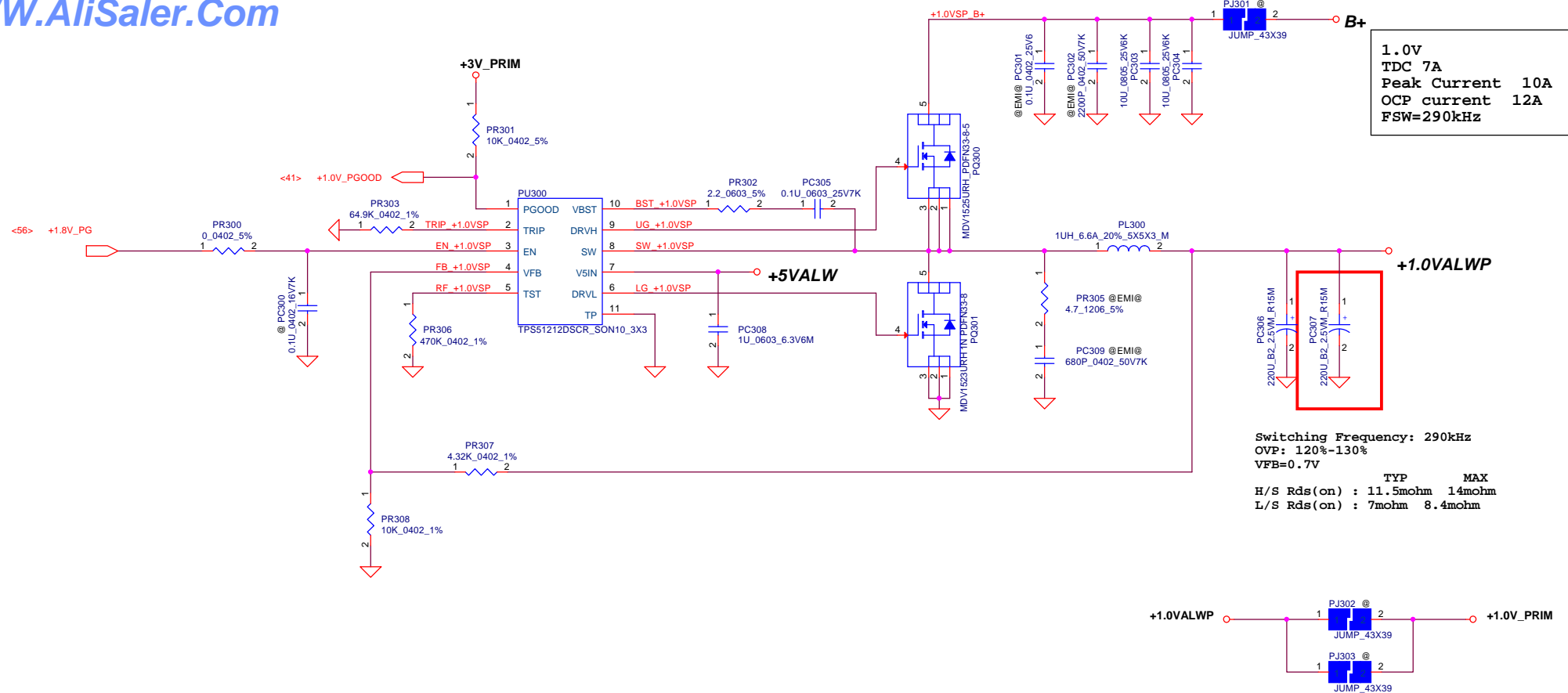


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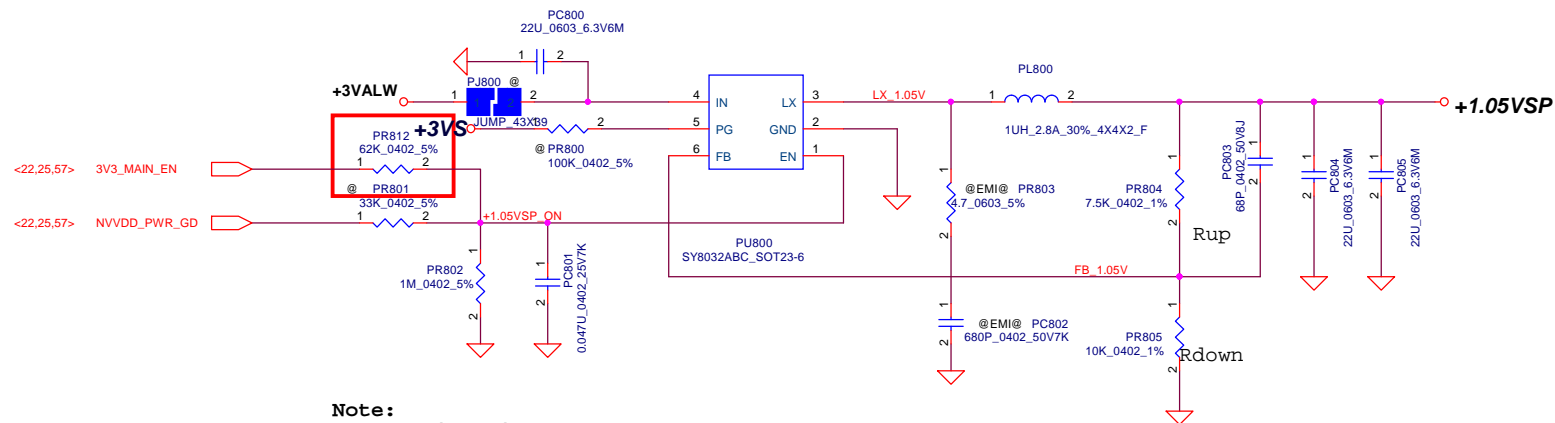
CC = 3.5A
CV = 17.7V
CP = 117W/19.5V = 6A
Hybrid trigger point = CP x 1.07 = 6.42A







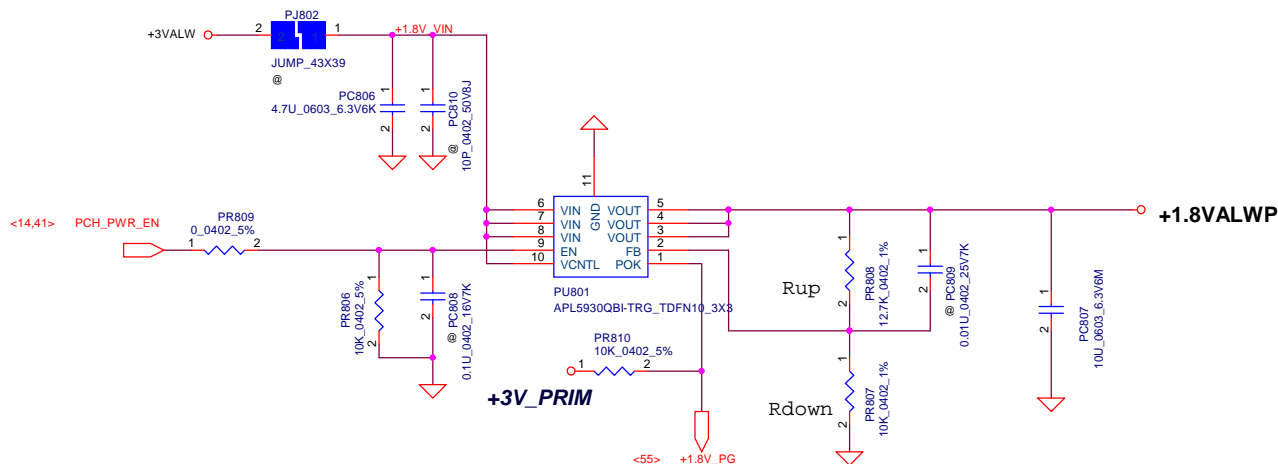
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/01/06	Deciphered Date	2016/01/06	Title	PWR-1.0VALWP
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1.05VSP
TDC 2A
Peak Current 2.9A
OCP current 3.5A
FSW=1MHz

Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

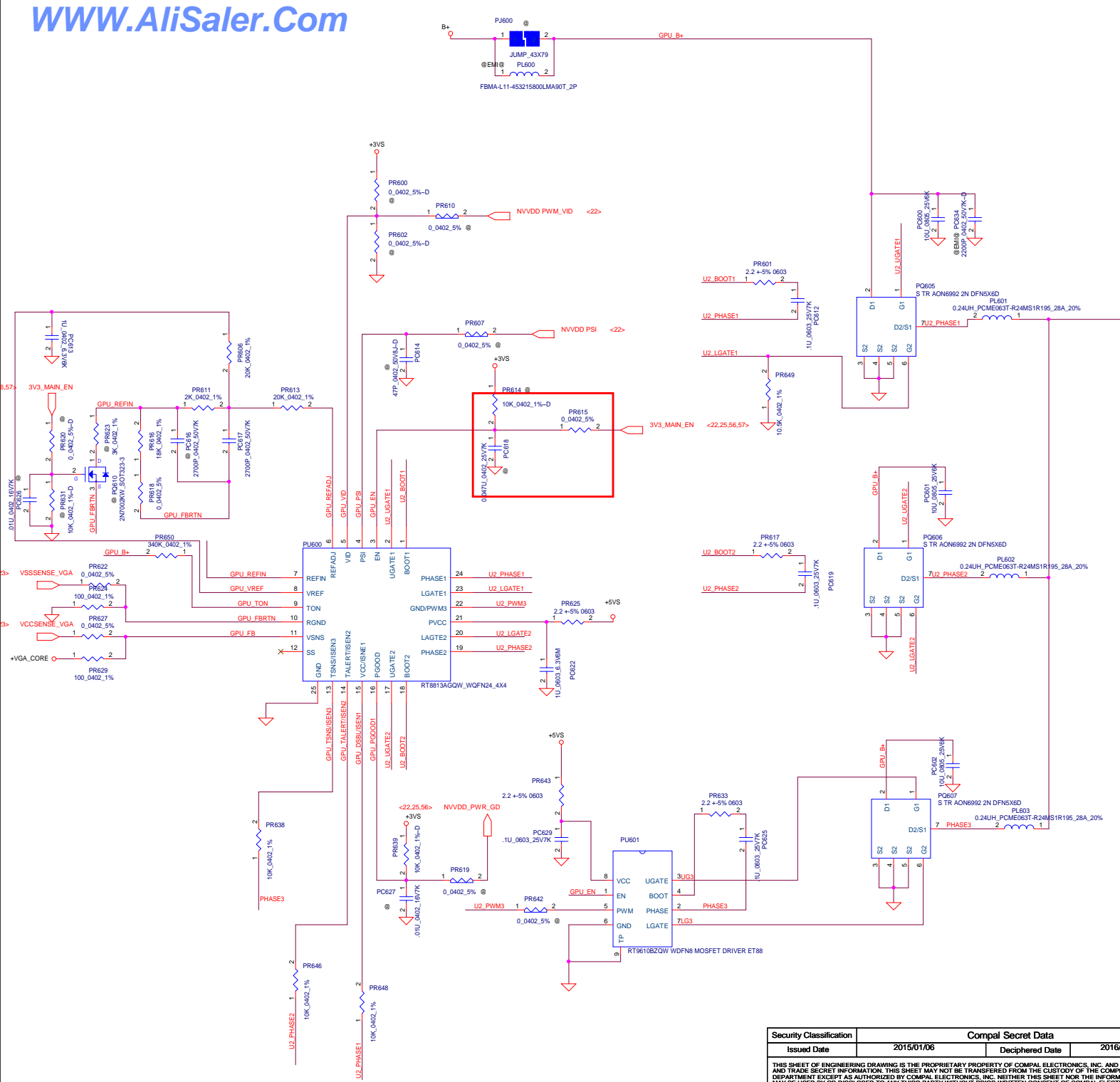
$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$



+1.8V_PRIM
TDC 0.27A

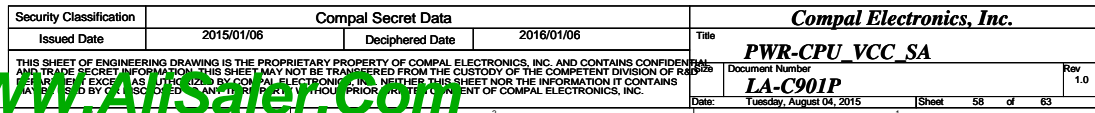
$$V_{out} = 0.8V * (1 + R_{up}/R_{down})$$

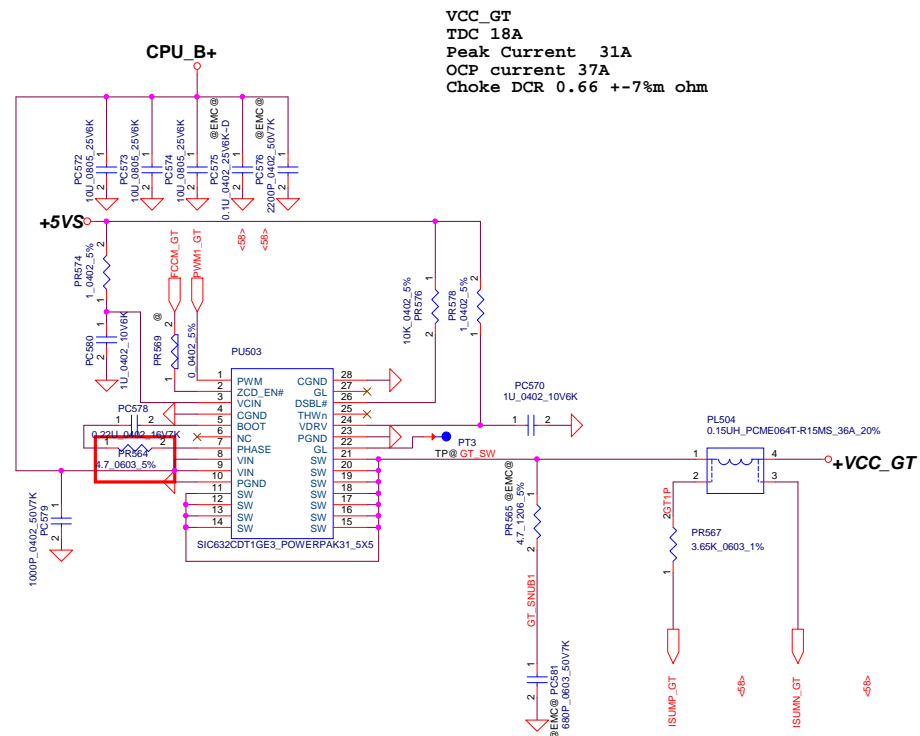
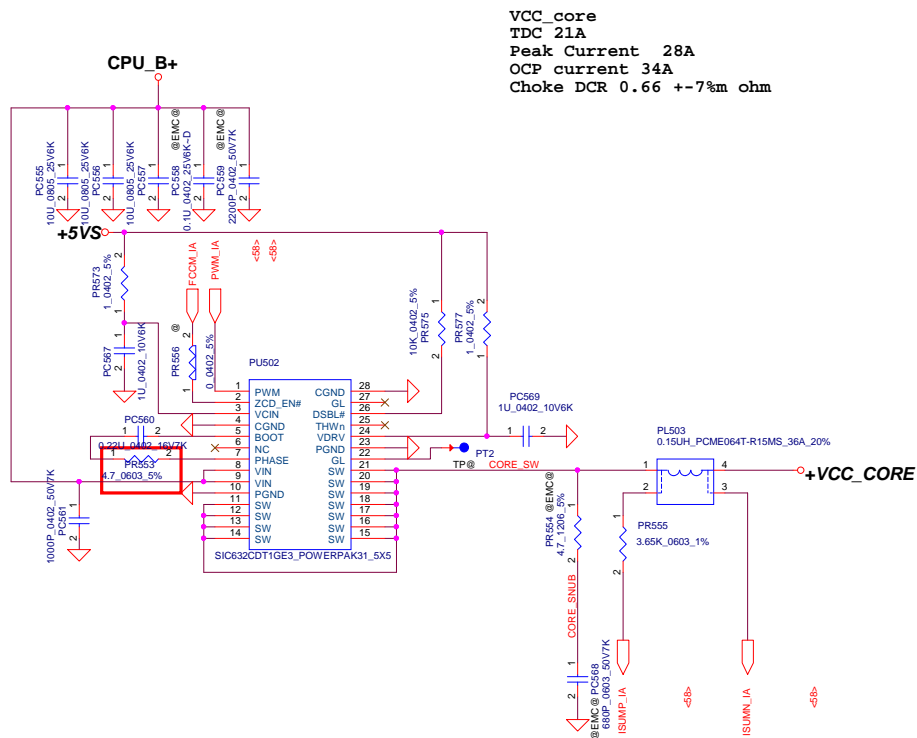
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/01/06	Deciphered Date	2016/01/06	Title	PWR-1.05VS VGA/1.8V PRIM
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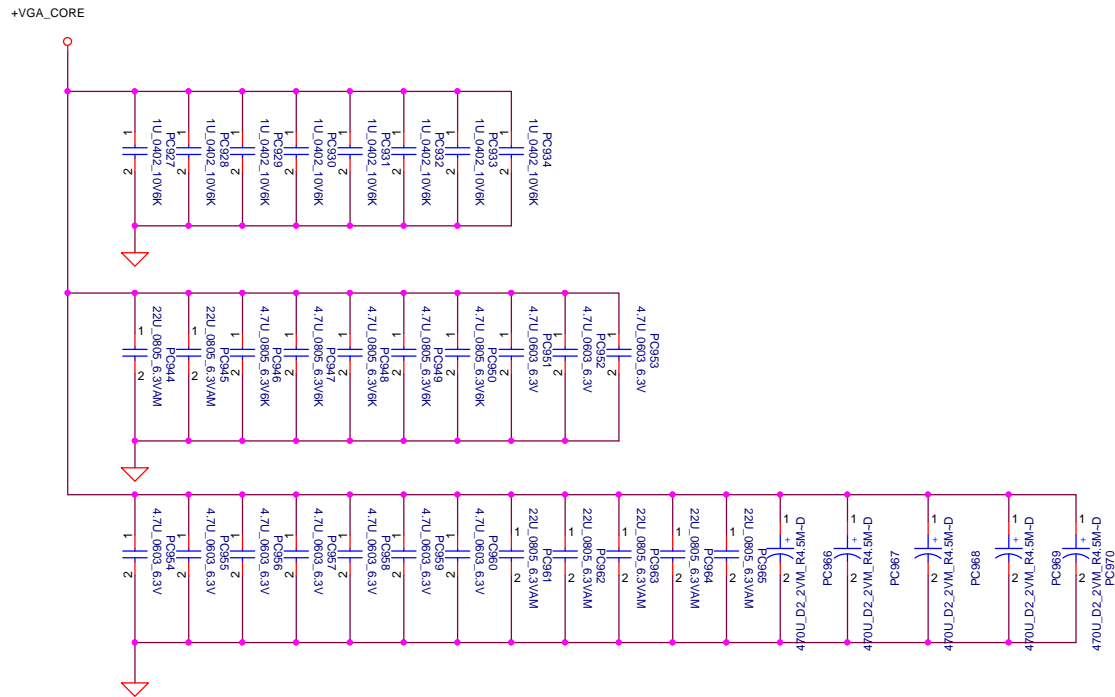


VGA_CORE
TDC 51.1A
Peak Current 87A
OCP=104A
TYP MAX
H/S Rds(on): 6.7mohm , 8.5mohm
L/S Rds(on): 1.8mohm , 2.3mohm

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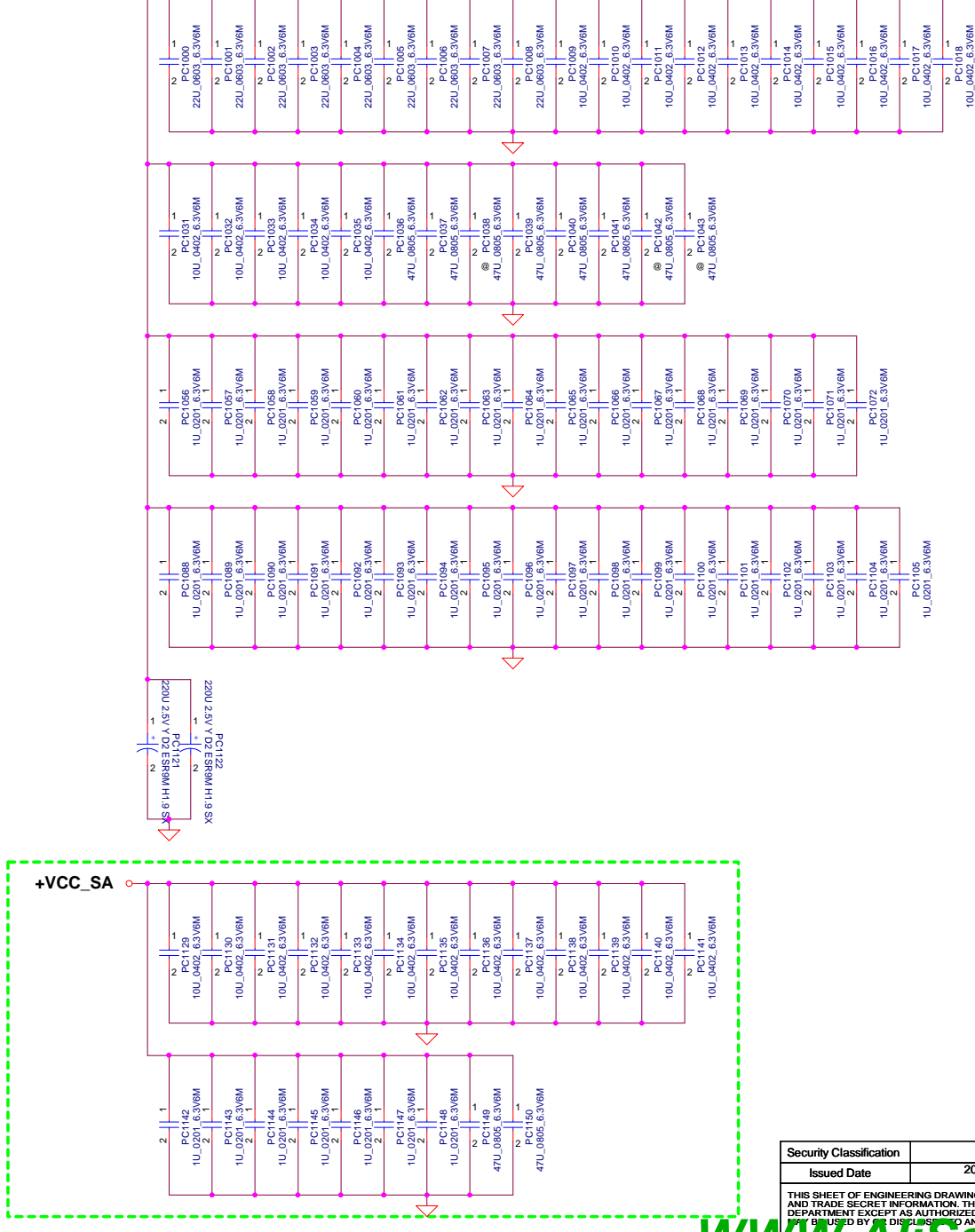




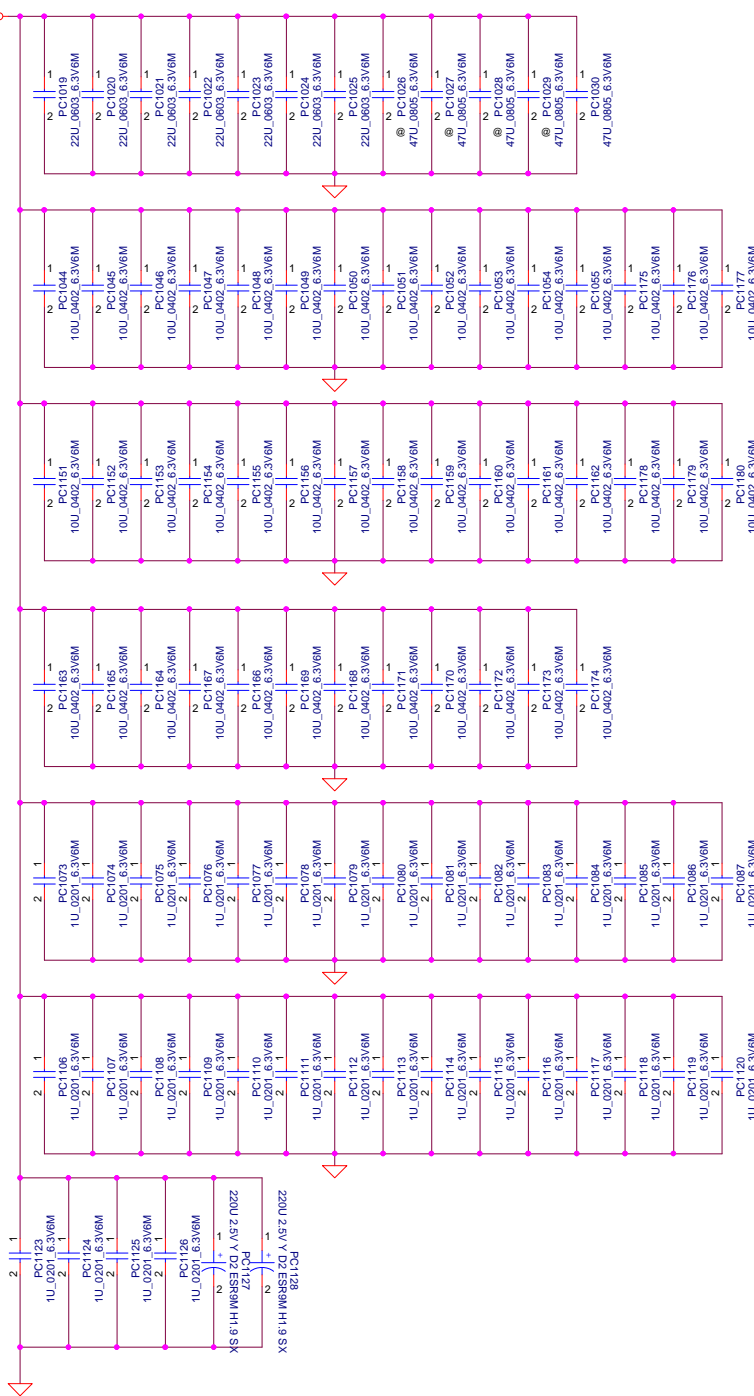


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+VCC_CORE

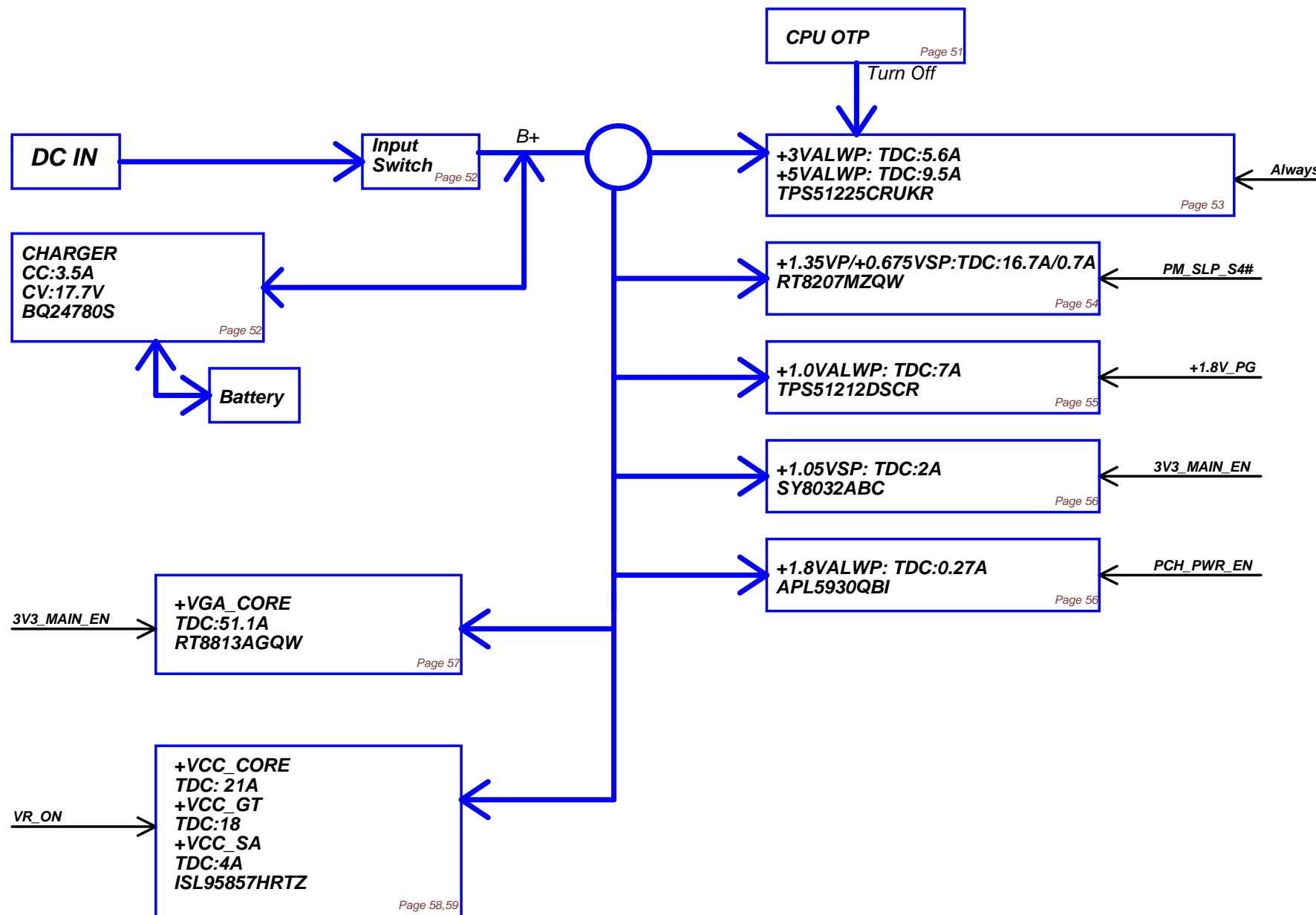


+VCC_GT



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Power block



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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	56	1.05VS_VGA	2015/3/6	Compal_PWR	For EE request to fine tune power sequence.	Change PR812 from 33k to 62k.	X01
2	57	VGA_CORE	2015/3/6	Compal_PWR	For EE request to fine tune power sequence.	Change PR615 from 33k to 0. Non-pop PC618.	X01
3	58,59	CPU	2015/4/1	Compal_PWR	For CPU transient and DC/DC EA fine tune.	Change PR550 from 2kOhm to @. Change PC547 from 680pF to @. Change PC543 from 0.01uF to @. Change PC527 from 0.01uF to @. Change PR552 from 2.61kOhm to 4.42kOhm. Change PR529 from 2.61kOhm to 4.42kOhm. Change PC516 from 2200pF to 1000pF. Change PR570 from @ to 20MOhm. Change PR553,PR564 from 2.2 to 4.7ohm	X01
4	54	1.35VP	2015/4/7	Compal_PWR	For EE request to fine tune power sequence.	Add PR210 to connect with PM_SLP_S4# , non-pop PR208.	X01
5	54	1.35VP	2015/4/8	Compal_PWR	For fine tune OCP.	Change PR201 from 8.06kohm to 10kom.	X01
6	55	1.0VALWP	2015/4/8	Compal_PWR	Improve output ripple voltage.	Add PC307.	X01
7	51	DCIN/BATT CONN/OTP	2015/5/20	Compal_PWR	For change CPU OTP point.	Change PR24 from 12.1k to 16.2k.	X04
8	51	DCIN/BATT CONN/OTP	2015/7/8	Compal_PWR	For cost down removed baed	remove PL1,PL2,PL3	1.0
9	57	VGA_CORE	2015/7/8	Compal_PWR	For cost down change baed to jumper	Add PJ600	
10	53	3.3VALWP	2015/7/8	Compal_PWR	For cost down removed baed	remove PL101	
11	56	1.8V_PRIM	2015/7/8	Compal_PWR	HW didn't need this. remove PR811	remove PR811	1.0 1.0

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